2026 ASEE ANNUAL CONFERENCE June 21–24, 2026 | Charlotte Convention Center, NC
Host Sponsor UNC Charlotte
ASEE AMERICAN SOCIETY FOR ENGINEERING EDUCATION
Paper ID #52054

A Semiconductor Nanotechnology Manufacturing Laboratory Course for First-Year Undergraduate Students

Jerry Austin Yang, Stanford University

Jerry A. Yang is a doctoral student and graduate research assistant at Stanford University pursuing a PhD in Electrical Engineering and a MA in Education. He received a BS in Electrical Engineering from the University of Texas at Austin with a certificate

Tara Pena, Stanford University
Swaroop Kommera, Stanford University
H.-S. Philip Wong, Stanford University

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Jerry A. Yang, Tara Peña, Swaroop Kommera, H.-S. Philip Wong
Stanford University

Abstract
Advancements in generative artificial intelligence, high-performance computing, and data centers require significant investment in semiconductor manufacturing and developing the workforce to support the semiconductor industry. However, most technical semiconductor classes are offered primarily to upper-division undergraduate engineering students, and more work needs to be done to expose a wide range of first-year undergraduates to the semiconductor field, its technical roots, and its wide-ranging impacts. Here, we develop a first-year introductory laboratory course in semiconductor manufacturing to address this need and implement it in Winter 2025 at a mid-size private university near Silicon Valley on the west coast United States. We present the course structure, learning objectives, and rationale behind the course design as well as student and instructor reflections on the course after it concluded. Our course design presents a path for other engineering departments to consider potential ways to incorporate nanotechnology laboratory experiences into first-year undergraduate curricula as well as foster a pipeline to prepare undergraduate students to enter the semiconductor industry workforce. By prioritizing students' engagement with real-world cleanroom facilities and semiconductor process engineers, we create impactful in-roads for students to connect with nanotechnology beyond the classroom.

Keywords: semiconductor, nanotechnology, first-year engineering education

Introduction

With the global surge in chip demand, the semiconductor industry faces a severe talent shortage, with some estimates projecting more than 58% of semiconductor manufacturing positions going unfilled by 2030 [1]. To respond to this need, recent efforts to stimulate the semiconductor industry in the United States, such as the CHIPS and Science Act, have also called for allocating resources toward developing the semiconductor workforce. However, semiconductor and nanotechnology education remains significantly understudied, and it is necessary to develop pipelines to introduce and prepare students early in their undergraduate education for future nanotechnology industries.

In this work, we present a design for a first-year undergraduate-level introductory nanotechnology course offered at a private, mid-size research university on the West Coast. The course is designed as a laboratory course with three key goals. First, the course aims to expose first-year students from *both* technical and non-technical backgrounds to the semiconductor manufacturing industry through hands-on in-class activities, cleanroom facility tours, guest speakers, and lectures. Second, the course seeks to contextualize the content with broader history of and trends in the semiconductor industry, raising key issues of economy, sustainability, and equity. Third, the course seeks to spark interest in semiconductors and encourage students to enter nanotechnology fields broadly.

Relevant Literature

Laboratory experiences are crucial to the professional formation and education of engineers [2]. Laboratory-based coursework has been thoroughly explored in a variety of science and engineering fields, from mathematics and physics to biological sciences. In many science and engineering programs, laboratory-based coursework is valued for its multifaceted role in developing experiential knowledge in students, giving students opportunities to have hands-on experiences, having students simulate "real-world" scenarios that professional scientists and engineers encounter, and ultimately, equipping students with better knowledge to enter the engineering workforce [3].

Semiconductor education presents a unique venue for laboratory-based coursework because of the interdisciplinary nature of the field and the concentration of laboratory resources into large-scale shared user facilities. At universities, semiconductor laboratory research and education are often centered around shared cleanroom fabrication facilities, where students and researchers from many different disciplines use the same tools and share knowledge about real-time tool issues, tool-specific technical procedures, process challenges, and practical hands-on informal knowledge that may impact many different facility users. These laboratory sites become working *communities of practice* for semiconductor processing, where students and researchers can engage and learn from each other in an educational setting [4].

Semiconductor fabrication laboratory courses emerged in the 1950s-60s in response to the rapid technical advancements in the field during World War II and significant demand for highly skilled workers in microelectronics manufacturing. As early as 1973, there were over 30 well-established university cleanroom fabrication facilities across the United States that were also used for semiconductor education [5]. Studies in semiconductor engineering education have focused primarily on best practices for laboratory course design [6], [7], interdisciplinary knowledge development and teaming/collaboration [8], [9], and adaptations to COVID-19 [10].

However, we observe that most semiconductor fabrication courses are primarily restricted to upper-division and/or graduate students due to operational and safety concerns [1], [5]. This curricular timeline is in stark contrast to other areas of engineering such as circuit design, where hands-on laboratory experiences are often introduced as early as possible, and limits possibilities for authentic semiconductor laboratory experiences within cleanrooms and adjacent laboratory environments. However, as semiconductor researchers and instructors, we believe that it is possible and necessary to introduce interested engineering undergraduates to hands-on semiconductor manufacturing as early as their first year to reap the benefits of such an experience. The integration of first-year students into dynamic working cleanroom fabrication facilities, engaging with real staff/researchers and real processes and tools, presents rich opportunities for interdisciplinary learning beyond a traditional classroom laboratory.

In this work, we leverage our positionality as active semiconductor researchers and cleanroom staff members to design a relevant and timely semiconductor engineering laboratory course for first-year engineering students at a medium-size private university in the United States. Our guiding questions for the course design were:

1. How can we design a semiconductor fabrication laboratory course that is accessible to first-year undergraduate students, assuming no prerequisite technical knowledge of the field?
2. How can non-technical (*e.g.* economic, social) broader impacts be incorporated into semiconductor courses to better contextualize students' experiences work within real-world challenges and provide means to discuss equity, ethics, and social justice issues in industry?

Our course design specifically draws on the shared staff knowledge and resources in our university cleanroom facilities. We strive to immerse students as fully as possible in the cleanroom, having them participate in lab demonstrations with experienced facility users as well as design their own silicon pieces to be taken home as course souvenirs. While we cannot provide true authentic, student-driven laboratory experiences due to logistical and safety concerns, we discuss ways we promote student engagement within the facility through the course. In addition, we highlight ways we incorporate equity-centered conversations into the classroom. We conclude with student perspectives and instructor reflections on the course.

Course Design and Implementation

Course Overview

Our course is designed for first-year undergraduate students at a medium-sized private university on the west coast of the United States, near Silicon Valley. The course is a seminar laboratory accommodating 20 students. To enroll in the class, students apply through a form directly to the faculty instructor. The faculty instructor selects students from various backgrounds to compose a diverse class with respect to student identities and (technical and non-technical) interests. The course is taught once a year in a 10-week quarter, meeting twice a week for 80 minutes. Laboratory sessions are held during class meetings and are entirely self-contained within the session. The course has been offered since 2015 but was redesigned for the Winter 2025 offering to clarify learning objectives, update/modernize curriculum, include broader impact discussions, and incorporate evidence-based teaching practices such as exit tickets and grading rubrics [11].

Course Objectives and Rationale

We outline and provide rationale for our course learning objectives. To construct the learning objectives, the teaching team started with the question, “What do we (as instructors) want students to take away from the course?”. After discussion, we converged on the following list in Table 1. Each objective is accompanied by a brief list of course content targeting the learning objective, which is elaborated below. We elaborate on each objective in the subsequent paragraphs, grouping related objectives for brevity.

Learning Objective *Students will be able to…*	Course Content
LO1. Explain how a transistor works and its role in modern computing systems.	Lecture 1
LO2. Describe the six basic semiconductor fabrication process modules and discuss how semiconductor process engineers combine them to design a fabrication process for transistors.	Lectures 2-3, Labs, Homeworks
LO3. Design a transistor in the lithography mask layout software KLayout.	Homeworks
LO4. Interpret basic semiconductor process flows and sketch plan-view and cross-section views of wafers based on a process flow.	Lectures 2-3, Homeworks
LO5. Discuss how semiconductor process engineers use design rules and process windows to ensure that processes work reliably.	Lecture 4, Labs, Homeworks
LO6. Describe how transistors are characterized and tested.	Lecture 5, Labs
LO7. Identify current trends in semiconductor and/or processing technology related to a field of your (students’) interest.	Guest Speakers, Final Project
LO8. Discuss some of the broader (environmental, social, economic, geopolitical) impacts of the semiconductor industry on society.	Lecture 6

Table 1. Course learning objectives and associated content.

1. *LO1. Explain how a transistor works and its role in modern computing systems.*

Modern computing systems have undoubtedly revolutionized human progress since the invention of the first transistor in 1947 by William Shockley, John Bardeen, and Walter Brittain. By understanding what a transistor is and how it operates, we believe that students gain critical insight into physics behind how modern electronics works. We contextualize the course in the introductory lecture by reminding students of the impact that transistors have on their own lives, as well as how ordinary everyday electronics that they use are comprised of transistors. We introduce the levels of abstraction, starting from large-scale data centers and ending at the state-of-the-art 10 nm FinFET transistors.

A key component of this learning objective is to introduce students to the real "under-the-hood" physics of the transistor, which is necessary to understand semiconductor processing and transistor design choices in the laboratory components. While other courses may emphasize other elements such as the historical significance of transistors, we believe that a strong technical grounding in transistor physics and fabrication processes enables richer discussion and questions around both emerging trends in the field and the broader impacts of the semiconductor industry. For example, by understanding how transistors use electric fields to modify current flow for "switch-like" behavior, it is possible to discuss transistor miniaturization through Moore's Law and current areal density challenges at the nanometer scale.

2. *LO2. Describe the six basic semiconductor fabrication process modules and discuss how semiconductor process engineers combine them to design a fabrication process for transistors.*

Similar to the first learning objective, this learning objective seeks to survey and categorize the wide breadth and complexity of semiconductor fabrication processes. In both the lectures and lab sessions, we intentionally spotlight specific processes that are most relevant to semiconductor industry based on our current knowledge. By front-loading the lecture sections on general fabrication techniques, we scaffold the lab sessions to deepen students' knowledge with more specific, detailed information about our cleanroom's tools and capabilities. These processes are also reinforced through the homeworks, as students are expected to design basic processes based on a given cross-section or image.

We center fabrication process techniques for two key reasons. First, it reveals the hands-on processes behind how modern chips are made. Second, by illuminating the technical details behind semiconductor manufacturing, students gain a unique technical perspective that allows them to unpack the underlying economic and geopolitical structures that support the technical process innovations. For example, understanding the process of lithography helps students understand the technical value and geopolitical consequences of the $400 million investments by semiconductor foundries in extreme ultraviolet (EUV) systems developed by Dutch lithography tool supplier ASML. Such conversations are directly addressed during lectures.

3. *LO3. Design a transistor in the lithography mask layout software KLayout.*

To ensure that students get hands-on experience with transistor design, we incorporate layout design and software into the course through homework assignments. Students are expected to learn KLayout largely outside of class, with resources provided online for help. We design the homework assignments to build up students' knowledge of KLayout over the timeline of the course so that by the final homework assignment, they are able to design a basic local back-gated transistor and fabrication process. This "ramp up" is designed to coincide with specific lectures on

transistor design rules and process reliability concepts to ensure that students can tie certain processes and lectures learned in class to specific drawing tasks in KLayout.

Introducing students to KLayout serves three key purposes. First, it reinforces technical content from the previous objective. Second, it gives students agency to design something to be fabricated in the laboratory sections, giving them a "stake" in the laboratory process. Seeing their own designs being etched or patterned creates more memorable experiences compared to patterning an arbitrary mask. Third, and most importantly, it gives students graphical visualizations of transistors and fabrication process steps, forcing them to carefully visualize both plan-view and cross-section transistor designs and what processing step(s) need to be accomplished for each layer. Visualizing transistors in this way is a critical skill in the semiconductor process engineer profession. This skill is reinforced through the homework assignments, where they are asked to both design simple processes and sketch diagrams of simple layouts.

4. *LO4. Interpret basic semiconductor process flows and sketch plan-view and cross-section views of wafers based on a process flow.*

As discussed above, a key skill of semiconductor process engineers is the ability to combine (or "integrate") fabrication techniques into process flows to make something useful. This learning objective relies on students' abilities to synthesize and apply the information gained in LO2 and KLayout skills acquired in LO3 to propose their own process flows for existing or potential structures. Here, we emphasize the process flows needed to make industry-relevant basic test structures in addition to the transistor, including diodes, capacitors, and thin-film metal resistors. In using these simpler structures as test cases for process flow and KLayout design in homeworks, we are able to scaffold student knowledge so that they are prepared to design a full transistor and process flow by roughly halfway through the course.

5. *Discuss how semiconductor process engineers use design rules and process windows to ensure that processes work reliably.*

Current chips made with state-of-the-art commercial technologies require nanometer-level precision: a few tens of nanometers of misalignment on a wafer can cost semiconductor foundries millions of dollars. Compounded with the proverbial "5 9's" yield requirement (>99.99999% yield) for industrial semiconductor production lines, process engineers must place stringent design rules and process windows to ensure process reliability across billions of transistors on a single chip. We introduce students to basic concepts behind design rules and process windows and discuss the role of process design kits (PDKs) and design rule checks (DRCs) in ensuring that device engineers can meet the transistor performance requirements for integrated circuit designers. During lab demonstrations, we address challenges in process uniformity and variability encountered in academic facilities compared to industrial production lines. Students are asked to apply various design rules based on our facility capabilities in their KLayout assignments. lluminating challenges of process reliability and yield is critical for students to understand process design choices on modern transistor technologies as well as the sheer scale and stringent process control at which modern chips are made.

6. *Describe how transistors are characterized and electrically tested.*

Throughout semiconductor processing, it is important to include process checks to ensure that each process step works as intended. In industry, characterization is crucial to cost-saving decisions and process control checks, leading to million-dollar impacts on the wafer scale. In the laboratory,

we demonstrate various techniques that semiconductor engineers use in academic fabrication facilities to check process outcomes and maintain process control. By highlighting the impacts of failed processes, we underscore the economic value of good design rules and process control in the multibillion-dollar industry.

7. *Identify current trends in semiconductor and/or processing technology related to a field of your (students') interest.*

Students are encouraged to explore how nanotechnology writ large relates to their interests and lives through the final project and selected guest speakers. The final project is discussed below. We identify guest speakers by collecting a list of student interests on the first day and selecting broad areas of interest that encapsulate most students' interests. These interests are used to select speakers from the cleanroom community of practice, with an emphasis on providing diverse and/or marginalized student perspectives to the class. The guest speakers are asked to focus on both their technical research and how they got into their lines of work. Providing this focus invite students to consider multiple potential career intersections between semiconductors and their own lives.

The final project acts as an opportunity for students to synthesize the information in the course and apply it to analyze real-world emerging technologies. While the instructor team's primary backgrounds are in semiconductors, applications of semiconductor processing range from biotechnologies to quantum computing to astronomy. Because the class population is general and not engineering-specific, this invites voices and perspectives from other areas of students' interests and pushes students to think outside of the course content.

8. *Discuss some of the broader (environmental, social, economic, geopolitical) impacts of the semiconductor industry on society.*

The semiconductor industry has a rich history in Silicon Valley, providing a source for economic and environmental transformation. While broader impacts are discussed at various points in the course, Lecture 6 focuses primarily on elucidating the hidden environmental justice and socioeconomic battles throughout the semiconductor industry's growth and maturity in Silicon Valley through the late 1900s. We draw on both primary sources, including local newspaper articles and historical toxic waste site maps, and secondary academic sources such as Pellow and Park [12], to initiate conversations around the environmental impacts and racial/gender stratification at the height of the semiconductor industry in Silicon Valley [13]. An in-class gallery walk activity helps categorize and evaluate the multiple impacts semiconductors have had. Students are also asked to engage with these consequences in their final projects as well.

We include this learning objective to illuminate the hidden narratives behind the massive technological leaps in the semiconductor industry during the late 20th century. Most technical semiconductor courses focus on the various technical innovations made in semiconductor processing during this time but do not cover the impacts these technical innovations had on toxic waste management and workers' health/safety rights. By 2003, there were ~25 federal toxic waste sites within a 10 mile radius of San Jose, primarily located in/near lower-income housing areas [12]. These stories centering marginalized peoples' experiences within the semiconductor industry's sphere of influence and critiquing the semiconductor industry's impacts challenges the dominant narrative within semiconductor classrooms that semiconductors' technological innovations do not come with social tradeoffs. By introducing students to these narratives, particularly situated in their local context, they can better assess the human impacts of new semiconductor technological innovations.

Compared to other first-year courses in science and engineering fields, we intentionally design this course with an epistemic value of scientific and technical significance. In other words, we purposefully forefront the technical knowledges behind transistor and process design, as opposed to socioeconomic or geopolitical impacts of the semiconductor industry, in our course design. We acknowledge that this perspective in engineering courses traditionally minimizes the broader societal impacts of technology, particularly hiding the social institutions that create social and environmental injustices. However, by presenting a clear picture of the technology from an engineering technical perspective, by the end of the course, we believe we provide students with a unique specialist perspective on the semiconductor industry's internal machinations that empowers them to critically assess the industry's societal impacts.

Course Timeline and Pacing

The course timeline is organized into three parts, as shown in Table 2. Weeks 1-3 contextualize the course within current problems, introduce basic transistor operation and fabrication process techniques. Key prerequisite knowledge of transistor physics is covered. Laboratory work includes a safety tour that involves entering the cleanroom as well as an external cleanroom infrastructure tour. Weeks 4-6 focus on laboratory processing, with a discussion of design rules and process control in the lecture. Weeks 7-9 focus on imaging and characterization with a laboratory week and a lecture. Between weeks 4-9, guest speakers from different research backgrounds are scheduled for four lecture days for students to engage with members of the cleanroom community of practice and learn more about the wide range of work/research done with semiconductor processing techniques.

Week	Lecture Content	Laboratory Content
1-3	Lecture 1: Introduction, transistor history, transistor basic physics/terms Lectures 2-3: Semiconductor processing modules and process integration	1 week: safety training, infrastructure tour
4-6	Lecture 4: Design Rules Guest speakers: Novel semiconductor materials	2 weeks: Photolithography/CVD (1 week) Etching/PVD/liftoff (1 week)
7-9	Lecture 5: Transistor/fabrication characterization techniques (e.g. SEM, FIB, TEM, AFM, electrical) Lecture 6: Semiconductors and society Guest speakers: Student interests	1 week: Imaging and characterization
10	Student final project presentations	Wafers with personal designs cleaved in class and given to students as souvenirs

Table 2. Course pacing, topics, and timeline

Laboratory Session Structure

Laboratory sessions are structured as "show-and-tell" demonstrations of tools associated with specific process modules. For each process module, specific tools are selected for the students to see based on tool availability and process speed. Cleanroom facilities staff experts and senior graduate student researchers familiar with the tools discuss the key physics, tool operation, and industrial relevance of each process within the context of the tool. These demonstration leaders are carefully chosen for their tool expertise as well as their role in facilitating the working community of practice that is the cleanroom fabrication facility. By having students meet key players in the facility operations as well as a range of tool users, students are exposed to a range of experiences

and perspectives on how each process module and tool is used in both transistor fabrication and other fabrication-based contexts/research lines at the university.

During the laboratories, students participate in all safety gowning procedures to enter and exit the cleanroom. This includes wearing a full cleanroom suit with boots and double-layered gloves. While in the cleanroom, students are allowed to handle wafers, cleave dies from a wafer with a diamond scribe, use microscopes to look at wafers, and operate some tools (mainly microscopes) with supervision. They are also allowed to document and take pictures of their cleanroom experiences for posterity.

In addition, for their first homework assignment, students use layout software KLayout to design a simple design that is fabricated during the lab sessions. The designs are combined into a master design that is used in subsequent processing steps, where patterned dummy wafers are used as part of tool and process demonstrations. For example, to demonstrate a metal wet etch process, aluminum metal would first be evaporated onto a blank silicon wafer, which would then be patterned with the students' designs before the laboratory session. Then, during the session, the students would watch the patterned areas be etched with aluminum etchant. This allows students to tie their design choices as well as see the impact of design rules (given in the assignment description) on process outcomes. At the end of the course, students are given their self-designed chips as souvenirs.

Assignments, Feedback, and Evaluation

Students were evaluated through three main assignment groups: attendance and participation, homework assignments, and a final project/presentation. Attendance and participation included attending most lectures and all lab sessions, filling out end-of-lecture exit ticket surveys, and participating in in-class activities with submitted deliverables. We leveraged this structure to request student feedback on instructional activities and incorporate their responses into future class meetings. For example, exit tickets often included an area for students to write down something they are still confused about at the end of class. These confusions were addressed in the next lecture. Submitted in-class deliverables enabled us to quickly assess the class's understandings of key learning objectives for that lecture and respond through further guidance, either virtually or in person.

Homework assignments were used to reinforce learning objectives outside of class time. Homework 1, given in the first two weeks of the course, introduced students to KLayout, a semiconductor device design and layout software. Students were tasked with learning basic usage of KLayout and demonstrating their knowledge with a simple fun design that would be used later in the labs, targeting learning objectives LO3 and LO5. Homework 2, given after Lectures 2-3, was a more traditional assignment focusing on semiconductor processes and process development. Students were required to revisit each process module learned in class and identify steps in a process flow based on a process diagram. In addition, students were tasked to draw various plan-view and cross-section schematics based on verbally described process flows. These tasks targeted learning objectives LO1, LO2, and LO4. Homework 3 tasked students to design a full transistor using KLayout using provided design rules and process constraints. Smaller problems in the assignment, such as designing resistors and capacitors, were added to walk students through different parts of the layout design process. These problems scaffolded student understanding to ensure that they were comfortable using KLayout within the context of transistor design, targeting learning objectives LO1-5.

To engage students in an iterative process of learning from feedback, we implemented a homework resubmission policy. After student submissions were graded against a rubric and returned, students could make corrections to their homework submissions for half credit back. This policy was originally developed for Homework 1 to ensure that students had a patternable design for lab sessions but was extended to subsequent homeworks as a means for them to implement actionable feedback and ultimately reinforce their mastery of the learning objectives. Most students took advantage of this policy.

Lastly, the final project provided an opportunity to synthesize the information presented in class with their personal interests. In groups of four, students identified a current innovation in nanotechnology broadly and conduct a literature survey identifying key problems, technical solutions, and broader impacts of their proposed topic. Students presented their findings in a group presentation and a 20-page report at the end of the course. We provided students with a project rubric, outlining the specific kinds of broader impacts (namely, technical, economic, social, and environmental) of their technological innovations they should discuss in their final products. Students were encouraged to interview experts in their field and follow up with research-backed conclusions. The final project addresses learning objectives LO7-8.

Student Perspectives

Methods

We collected student feedback throughout the Winter 2025 course offering to evaluate students' achievement of our stated learning objectives and student perspectives on the course structure. We use post-class surveys and an end-of-course survey. Surveys included a mixture of Likert-style questions, ranking questions, and open-ended questions for students to reflect on specific aspects of the class. Our study was approved by the institutional IRB, protocol #78622. We collected informed consent from the students prior to data analysis.

A third-party researcher managed recruitment, data collection, and data deidentification for the study to ensure that the teaching team did not influence students' consent to participation in the study. The researcher attended the two lecture sessions in the penultimate week of the quarter and presented a short description of the study at the end of class. Informed consent forms were distributed and collected in class. In addition, the researcher sent an email to the students reminding them of the study on the last week of class in case some students were not in attendance for both lecture days. Our resulting sample size was nine students.

Student Perspectives

Overall, students expressed having a strongly positive experience taking the course. Of the five students who completed the final course survey, three mentioned that they were seriously considering nanotechnology as a potential career path, and all students noted that their motivation to pursue engineering was significantly increased because of the class. When asked to rank the course elements they found most helpful in achieving the learning objectives, students ranked the labs the most helpful by far, followed by the guest speakers and homework sessions.

The key highlight for most students was the lab sessions. Students felt that some lectures were more abstract and harder to follow, but lab sessions were opportunities to revisit and reinforce the theoretical knowledge they gained at the start of the course. They also enjoyed gowning up in bunnysuits as well as talking to the various lab demonstrators to learn more about their specific applications and work. These conversations eventually led to out-of-course connections where the students were able to get more involved in lab research.

On the flip side, students sometimes struggled with the course pacing in the labs. Since the course structure frontloaded all the process modules/integration in two lectures at the beginning of the quarter, students expressed difficulty remembering and/or making connections with the lecture concepts during lab. One student proposition was to restructure the course in a more "just-in-time" structure with respect to the labs, where only key processes and tools would be covered the lecture before the respective lab week.

Students enjoyed other elements of the course, including designing their own layouts in KLayout. Students noted that using KLayout, particularly on homeworks, provided opportunities to apply design concepts taught in class rather than merely regurgitating content. While homeworks were challenging, students found them often worthwhile learning experiences beyond the classroom. On average, students reported spending less than 5 hours on learning KLayout, indicating that incorporating it did not increase their cognitive load. Students also appreciated the multiple chips they could keep at the end of the quarter as souvenirs.

One major critique students had was the sheer amount of technical jargon to overcome. While students became more comfortable with general cleanroom processing terms throughout the class, it was difficult for some students to remember more niche or detailed terms from lecture in the labs, for example those specific to a process module (*e.g.* conformality or isotropy). The complexity and density of new terms, particularly for first-year undergraduates approaching nanotechnology for the first time, is a persistent challenge in our course that we have sought to mitigate, as described in the next section.

Instructor Reflections and Next Steps

After the class, we reflected on the affordances and challenges of the course structure and brainstormed key changes to make for the next course offering. First, a key advantage of the course structure was front-loading a lot of fundamental core material early so that students understood the lab session demonstrations. While this structure scaffolded the remainder of the quarter, the significant cognitive load of having students digest many essential concepts quickly meant that students did not get a chance to absorb the material until the homework assignments or lab sessions, which could be up to six weeks after the lectures. This tension between lecture and assignment pacing led to discussions on ways to continually encourage student engagement in early content throughout the quarter.

Second, providing students rubrics and clear outlined instructions for their final project was a significant change from previous iterations of the course based on evidence-based teaching research and significantly improved the overall quality of the final project presentations. Previous course offerings primarily assessed student projects based on how well the instructors felt they met the assignment requirements and broader learning objectives, with minimal feedback to students on what the instructors were looking for. By formalizing the assignment into a clear, concise document with specific instructions, as well as providing a specific rubric with clear grading categories and standard, students were able to produce projects that clearly met the specific grading criteria and objectives for the project.

Third, the homework resubmission policy was a significant success, as students often took the opportunity to cross-check their work with other students and/or come to instructor office hours to review their work. These opportunities for course engagement allowed us to increase dialogue with and check in on specific students when needed. Finally, the implementation of end-class exit surveys introduced new modes of collecting real-time student feedback and overall feelings on course content. As mentioned above, this avenue of feedback enabled us to be more responsive to

student needs and revisit content that students found difficult in subsequent lectures. Previous iterations of the course did not have exit surveys.

We also encountered persistent challenges throughout the course. First, due to the depth of detail that semiconductor processing can achieve, it was difficult to contain the content of the course to key essential knowledges to prevent student cognitive overload, particularly during the first two weeks of the course. We discussed multiple options of removing various content, debating what content needed to be covered in lecture and what content could be moved to the homework, so that students could still be exposed to it without taking class time. We decided that process integration required a fundamental understanding of individual process modules, pushing process integration ideas to the homework for students to engage with as an exercise in deepening their understanding of individual process modules. We also sought to reinforce early concepts throughout the quarter by designing the homework assignments to build on previous assignments.

A second challenge we encountered was that lab sessions tended to be very chaotic, particularly with shuffling students through the gowning process and moving them to the correct locations in the cleanroom. Since the cleanroom space is confined, we divided students into four groups of five and rotated the groups between the demonstration stations, with ~30-40 minutes per station. Each week contained four lab demonstrations, so that all groups could see all demonstrations within the week. This organization was facilitated with multiple staff and volunteers asked to help with the course. In addition, checking attendance and participation during lab sessions was often difficult due to the chaotic nature of having students put on full cleanroom suits and maneuvering them around the cleanroom to specific demonstration locations. This procedure also reduced the lab time per session by 10-15 minutes, as students needed time to suit up before the lab session started. Generally, most students appeared engaged and willingly participated in in-class/lab activities. We have not been able to determine a better logistical solution to this problem – a solution would potentially enable us to increase the class size and reach more potential future semiconductor engineers.

For the next course offering in Winter 2026, we made a few key changes to the course structure. First, for the lectures labeled in Table 2 (except for guest speakers), we created short digital handouts summarizing key information, technical jargon, and takeaways accompanying the lectures, intended as a quick reference sheet for future homework or beyond the course. An example snippet is provided in Appendix A. The handouts were edited with blanks and then given to students in class to fill out during the lecture. The handouts were completion grades included in students' overall attendance and participation grade. If students missed a lecture, they could get the material through looking at online posted slides. This additional assignment adds another point for student entry/engagement of the material, as they need to review the lecture slides to complete the handout.

Second, based on student feedback that the first two lectures were very abstract, we switched the order of the first lab week and Lectures 2-3 for the Winter 2026 course offering. This switch meant that students did an initial tour of the cleanroom facilities before learning about specific processing techniques. Initial student feedback has been very positive, with some students noting that seeing the physical space first helped tie conceptual elements of the lecture to specific parts of the tour.

Conclusion

We developed a semiconductor fabrication laboratory course for first-year undergraduate students at a medium-size private university located near Silicon Valley in the United States.

Through cleanroom process and tool demonstrations, our course provided a unique experience for first-year students to engage in a laboratory community of practice, dialogue with researchers using the facilities, and explore their own interests with respect to nanotechnology. Students developed their knowledge on transistor device physics, manufacturing processes, design rules, and process control. In addition, students were introduced to broader impacts beyond economic and geopolitical narratives of chip manufacturing, highlighting environmental and social justice issues that the semiconductor industry has created. Our course structure opens avenues for dialogue on providing exposure to semiconductors and nanotechnologies early in undergraduate engineering programs, supporting the pipeline for future semiconductor engineers.

Acknowledgments
This work was completed at the nano@stanford fabrication facilities, RRID:SCR_026695.

References

[1] Y. S. Sun, Q. Zhu, and J. M. Case, "Preparing Future Semiconductor Talent in the Global Context: A Comparative Study of the Semiconductor Engineering Curriculum in the US and Taiwan," presented at the 2024 ASEE Annual Conference & Exposition, Jun. 2024. Accessed: Sep. 11, 2024. [Online]. Available: https://peer.asee.org/preparing-future-semiconductor-talent-in-the-global-context-a-comparative-study-of-the-semiconductor-engineering-curriculum-in-the-us-and-taiwan

[2] National Research Council, *Educating the Engineer of 2020: Adapting Engineering Education to the New Century*. The National Academies Press, 2005.

[3] L. D. Feisel and A. J. Rosa, "The Role of the Laboratory in Undergraduate Engineering Education," *J. Eng. Educ.*, vol. 94, no. 1, pp. 121–130, 2005, doi: 10.1002/j.2168-9830.2005.tb00833.x.

[4] E. Wenger, "Communities of practice and social learning systems," *Organization*, vol. 7, no. 2, Art. no. 2, 2000, doi: 10.1177/135050840072002.

[5] J. M. Feldman, "Semiconductor Device and Integrated Circuits Laboratories: A Survey of Current Educational Practice," *IEEE Trans. Educ.*, vol. 16, no. 1, pp. 2–10, Feb. 1973, doi: 10.1109/TE.1973.4320780.

[6] B. Senitzky, "A Semiconductor Technology Course," *IEEE Trans. Educ.*, vol. 23, no. 4, pp. 213–218, Nov. 1980, doi: 10.1109/TE.1980.4321419.

[7] R. D. Engelken, "Innovations in undergraduate engineering education through NSF ILI- and NASA JOVE program-sponsored development of a laboratory course sequence in semiconductor materials," *IEEE Trans. Educ.*, vol. 40, no. 4, pp. 259–265, Nov. 1997, doi: 10.1109/13.650838.

[8] A. J. Muscat, E. L. Allen, E. D. H. Green, and L. S. Vanasupa, "Interdisciplinary Teaching and Learning in a Semiconductor Processing Course," *J. Eng. Educ.*, vol. 87, no. 4, pp. 413–421, 1998, doi: 10.1002/j.2168-9830.1998.tb00373.x.

[9] C. Schindler, "Virtual Collaboration in a technical laboratory - an example from semiconductor technology," in *Teaching and Learning in Virtual Space*, wbv Media GmbH & Company KG, 2023, pp. 121–126.

[10] L. Chen *et al.*, "Semiconductor device fabrication lab demonstration during and after COVID-19," in *Proceedings of the 35th Annual Conference of the Australasian Association for Engineering Education (AAEE 2024)*, Christchurch, NZ: Informit, Dec. 2024, pp. 1292–

1300. Accessed: Apr. 27, 2026. [Online]. Available: https://search.informit.org/doi/abs/10.3316/informit.T202503240001330197682985 6

[11] D. L. Schwartz, J. M. Tsang, and K. P. Blair, *The ABCs of How We Learn*. Norton Professional Books, 2016. Accessed: Sep. 25, 2024. [Online]. Available: https://wwnorton.com/books/The-ABCs-of-How-We-Learn/

[12] D. Pellow and L. S.-H. Park, *The Silicon Valley of Dreams*. New York, NY: NYU Press, 2002. Accessed: Oct. 08, 2024. [Online]. Available: https://nyupress.org/9780814767092/the-silicon-valley-of-dreams/

[13] G. A. Chen and J. Y. Buell, "Of models and myths: Asian(Americans) in STEM and the neoliberal racial project," *Race Ethn. Educ.*, vol. 21, no. 5, pp. 607–625, Sep. 2018, doi: 10.1080/13613324.2017.1377170.

Appendix A: Sample Handout Page

How does a transistor work?

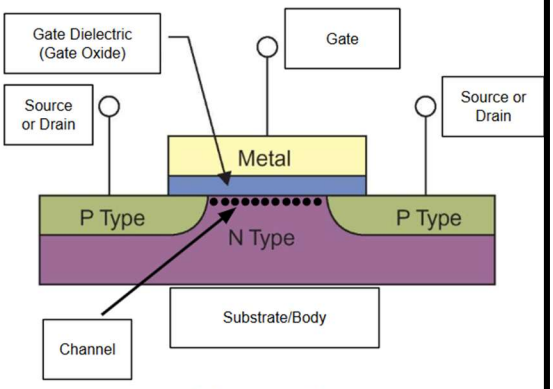
A transistor has 4 electrical terminals: gate, source, drain, and body/substrate. (The body is not always accessible.)

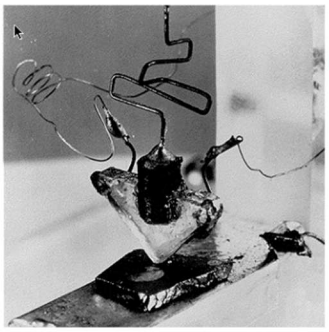
The most common analogy is of a switch or a faucet: when the gate (faucet handle) opens, charge carriers (electrons or holes) are able to flow from source to drain, creating a measurable current.

Instead of water and faucet handles, transistors use electric fields or voltages to control charge flow.

1. A voltage across the gate and source/body (V_{GS}) pulls charge into a thin layer under the gate dielectric, called the channel.
2. A voltage across the source and drain (V_{DS}) pushes the charge out of the device, creating current.

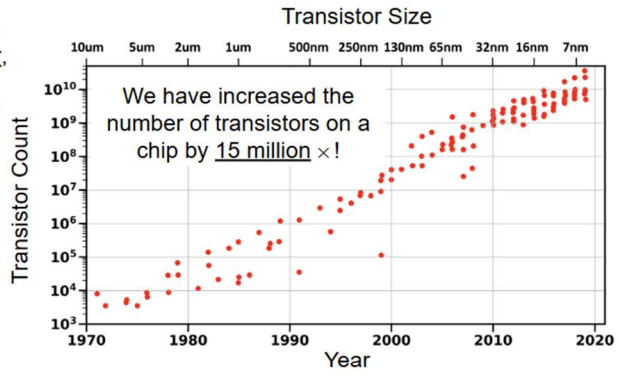
Parts of a (2D planar) transistor





First transistor, made in 1947

By making single transistors smaller, we can increase the complexity of each chip with more transistors.



In this course, we will focus primarily on how we make transistors. To make transistors, we can think of it as similar to cooking, where we need four basic elements:

Ingredients:
Silicon wafers, process chemicals, gases

Recipes:
Processes

Tools:
Wet benches, etc.

Facilities:
Cleanroom fabrication "fabs"

Why is semiconductor manufacturing so difficult?

- Transistors are small - only 10s of atoms wide
- Everything has to be precise
- Billions of transistors per chip, every one has to work
- Control dimensions down to 1 in 300 million