Outcome-Based-Competency-Focused Curriculum – Alliance Model 2025

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With an industry experience of about 6 years and 41 years of teaching and training, nationally and internationally acclaimed expert in outcome-based education (OBE), has been the pioneer of OBE in India since 1987. With considerable number of published national and international papers about the successful OBE researches undertaken at NITTTR Bhopal on a small and large scales are regularly cited across the world, both on engineering and non-engineering platforms. With more 5 books published, the latest 2024-OBE Handbook with NEP 2020 focus for Higher Education and 2021-OBE book for Engineering Education are the sought-after unique books. Two other books on wind power technology for the university systems and industry are equally popular text books in various universities. He has been a guest professor to various universities and professional Institutions in Europe, China, Africa and Asia.

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Abstract

This 8-page "Work in Progress" paper, with relevant examples in the annexures, is all about a novel industry-connected engineering education curriculum development model. Since the launch of the National Education Policy-2020 (NEP-2020) by the Government of India, the education systems are required to adopt the national mandate of "Competency-based Framework". This is a paradigm shift from the "traditional syllabus" to the Outcome-based Education (OBE) curriculum philosophy. But, knowingly or unknowingly, most universities exhibit only a superficial compliance to this national mandate. Their tinkered traditional syllabi are only "old wine in new bottles" as they are often disguised as OBE curricula with hardly any industry-connect. It is in this backdrop; the authors re-engineered the UG engineering programme curricula as the "Outcome-based Competency Focused Curriculum (OBCFC) Alliance Model 2025". The key takeaways from this conference are, understanding the scientific design of a typical OBE curriculum, "Outcome-Based Teaching-Learning (OBTL)" and "Outcome-Based Assessment (OBA)" for enhancing the employability.

Keywords: *NEP-2020, Industry, OBE, Outcome-based Competency Focused Curriculum (OBCFC), Learning Outcomes (LOs), Professional Competency, Course Outcomes (COs), Practical Outcomes (PrOs), Affective Domain Outcomes (ADOs), Learning Unit Outcomes (LUOs), Teaching-Learning (T-L), Micro-project*.

1.0 The Backdrop

Until the year 2020, the National Policy on Education (NPE) -1986 guided the Indian education system that aimed to promote equality, access, and quality in education. However, there was still a lack of uniformity in the education systems across the country resulting in several challenges. Hence, in the year 2020, the Government of India (GoI) launched the New Education Policy (NEP), now known as "*NEP-2020"* a game-changer [1] for the Indian education system from the primary to the doctoral level of education. *NEP-2020* aims to usher in uniformity across India by adapting the universally accepted OBE philosophy and also usher in parity with global standards.

Being a large country with diverse languages and cultures, the sudden breakaway to adapt OBE from the decades long traditional syllabi (see annexure-1) often with its emphasis on rote-learning continues to be a challenge, even after 5 years of NEP-2020 promulgation. Whereas, the focus of OBE is on the acquisition and display of LOs in order to raise employability levels. OBE requires a change of mindset in the teachers with respect to the varied instructional and assessment techniques; whereby adapting OBE became a herculean task for them. This backdrop spurred the authors to design and implement the *student-friendly* and *industry-aligned* Outcome-based Competency Focused Curriculum (OBCFC) "*Alliance Model 2025"* as a holistic and practical reengineering effort. Thus, history was created for by this University with the launch of this *Competency-based Framework* OBE curriculum model for their UG engineering programme offerings in the southern Indian state of Karnataka since July 2025 to benefit the country at large, or perhaps the whole world. The first batch of graduates from this OBCFC *Alliance Model 2025* is expected to emerge out in the year 2029.

2.0 Curriculum Scenario Post-NEP-2020 Promulgation

"The shift to OBE is so pronounced that, some education experts identify the shift to OBE and accreditation as one of the top 5 major changes in the last 100 years" [2]. In a large

country such as India, with more than 1,338 universities (including central, state, private, and deemed-to-be universities) and 68,680 Higher Education Institutions (HEIs), changing the mindset of the *teacher and the taught* about OBE continues to be a daunting task since the launch of NEP-2020. The pre-NEP-2020 "*traditional syllabi"* (see Annexure-1) in most Indian universities were *teacher-centered,* generally divided into 4 to 6 topic clusters called *modules* (or *sections*) with 4 to 6 academic "credits". In post-NEP-2020 scenario when OBE became mandatory, most universities added a few textbooks, tinkered the same teacher-centered *traditional syllabi* (in their ignorance or otherwise) and included a few casually framed "Course Outcomes" (COs) with hardly any industry-connect (see Annexure-2). The traditional *chalk and talk* teaching-learning (T-L) styles still continue in these HEIs with hardly any focus to develop and assess the attainment of the learning outcomes (LOs).

Even though most universities claim to be following the OBE philosophy, their practicums still continue to be *verification of theory* or *study type* experiments, that are irrelevant at the workplace/industry. Moreover, these experiments are often grouped as separate courses, disconnecting them from the related *theory courses*. Instead of assessing the attainment of LOs, they assess only the concepts and principles [see Annexure-3]. In other words, such so-called *OBE curricula* are only *old wine in new bottles*. They disguise their tinkered *traditional syllabi* as OBE curricula. Thus, most of the universities/HEIs exhibit a superficial compliance with the OBE philosophy pretending to align with the national mandate of *Competency-based Framework* [4], [5], [7], [8]. To onboard such institutions on to the common platform of *"Competency-based Framework"* for uniform OBE curricula, the GoI statutory bodies released the *National Guideline Documents* [4], [5], [7], [8], [9].

Thus, the *OBCFC "Alliance Model 2025"* (see figure 1) was scientifically evolved to incorporate the directives and guidelines stated in these *National Guideline Documents* to reflect the right ethos of OBE. The scientific process adopted in this curriculum design indicates the distinct specificity of the LOs flowing from left to right (see figure 1) i.e. from the broadly specified "Global-level *Goals* (i.e. PSOs)" till the "Micro-level *LOs* i..e. PrOs, ADOs, LUOs". The three pillars of OBE i.e. *outcome-based curriculum (OBC)* which is the *beating heart* of any educational programme, the *pedagogy* or *outcome-based teaching learning (OBTL)* and the *outcome-based Assessment (OBA),* are embedded in this novel model, as discussed in this paper, with examples in the annexures.

3.0 OBCFC Alliance Model 2025 and Professional Competency

"The United Nations Sustainable Development Goals present targets for 2030. Engineers are vital contributors for making progress towards these goals." [9]. The salary earned by a graduate is not for the knowledge/understanding that s/he possesses (as they are hidden in the brain) but, it is for *DOING* the various levels of jobs. These jobs in the industry could range from the micro-level to global-level defined as *micro-level, meso-level, macro-level* and *global-level* LOs by the academia. The foundation stone of every course is the *macro-level* LO i.e. ***Professional Competency*** [4], [6], [9] associated to the concerned occupation (see Annexure-4 and 5). This macro-level *Professional Competency* is equally understood by both academia and industry employer alike. It has several definitions; "Competence is a complex action system encompassing cognitive skills, attitudes, and other non-cognitive components" [10]. "Competence could be defined as the ability to undertake complex demands successfully or, to carry out an activity or task" [11]. "Traditional content-driven and time-based models of education are criticized as being too theoretical and for failing to meet the demands of practice, while newer ones based on skills and competency are called into question for being atomistic, controlling and confined to the predictable" [12].

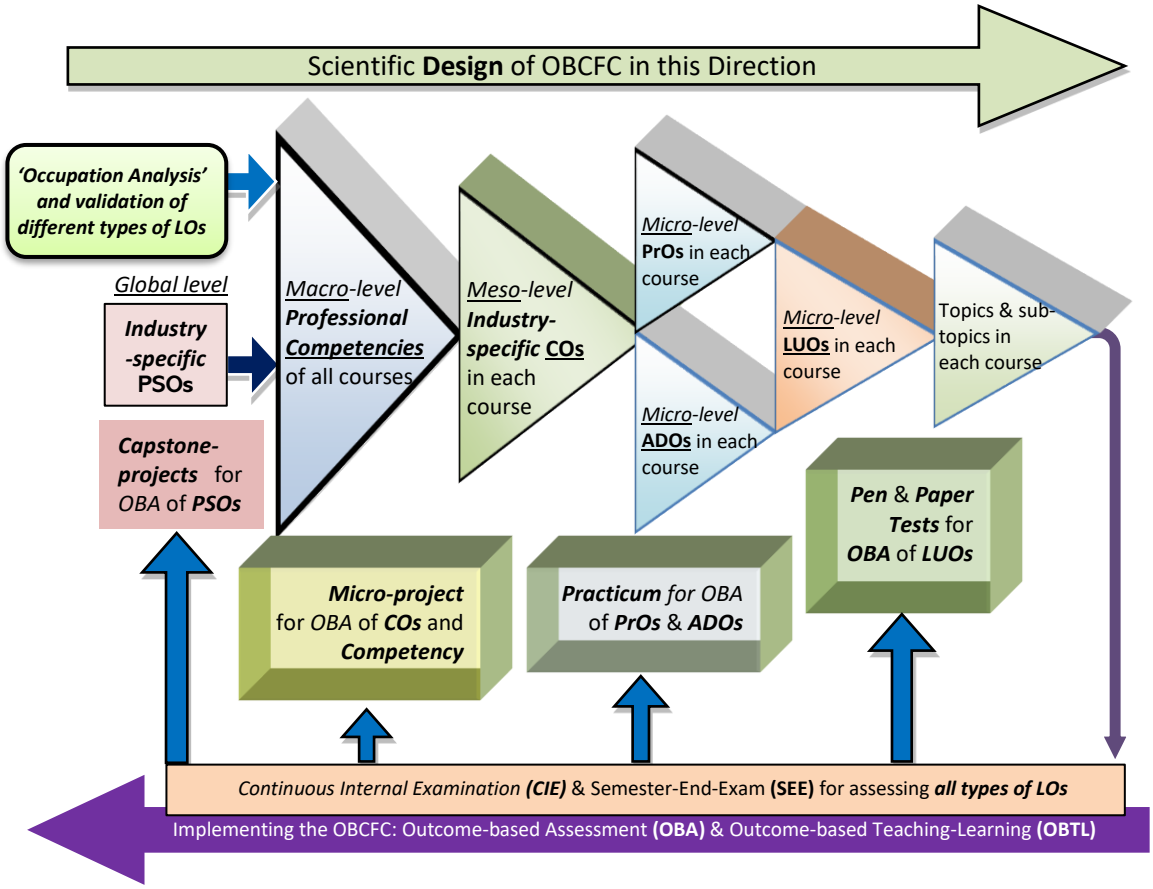


Figure-1. *Outcome-Based-Competency-Focused Curriculum "Alliance Model 2025"*

"The professional competence profiles for each professional category record the elements of competence necessary for performance of that the professional, is expected to demonstrate in a holistic way at the stage of attaining Registration" [9]. All these definitions indicate that the "Competencies stated at the macro-level are needed to fulfil the over-arching *Goals* and *Aims* of the concerned educational programme, that focus on both *personal* and *societal* development levels" [10]. Summarising these, the definition considered in this model is the most near to the industry expectations i.e. *"Competency is a statement that indicates the successful completion of a macro-level industry-specific main task at the threshold level, without hurting oneself, wasting raw materials, damaging any device, beginning with a SMART action verb of terminal nature consisting of a cluster of inter-related sub-tasks/skill-sets"* [13], [14], [15], [9], [16], [17]. Each *macro-level Professional Competency* is generally related to a particular *"course"* in a UG program, based on which, each *"Course Structure"* is built up in this OBE curriculum model.

4.0 Competency-based Framework and OBCFC "Alliance Model 2025"

For the smooth adoption of the *Competency-based Framework* by all educational institutions for aligning with NEP-2020, the Ministry of Education GoI have released orders for its compliance in order to produce work-ready graduates. It is a paradigm shift from the decades old teaching-learning (T-L) methods to the *Outcome-based Teaching-Learning (OBTL)* transactions and *Outcome-based Assessment (OBA)*. However, even today, most of the curricula in the Indian Universities continue to use their tinkered traditional *syllabi* (see Annexure-2) renamed as "OBE curricula" focusing only on the understanding of the topics. Whereas, the OBE curriculum has to focus not only on the understanding of the *topics,* but has to go still further to equip the students for acquiring the LOs required to ***DO*** the micro-

level to macro-level jobs in the industry. As the students' journey through each course every semester, they have to acquire the different types of LOs such as the *micro-level* LOs, *meso-level* LOs and the *macro-level LO* i.e. *Professional Competency* (see figure 2 and Annexure-4). The combination of the *Professional Competencies* builds up the *global-level* LOs i.e. PSOs. The unambiguously stated industry-specific LOs in this model motivate the students for self-learning too, whereby, the role of the teacher shifts to more of a *facilitator* of the T-L process for acquiring these LOs also the *assessor* of the students who have the attained LOs.

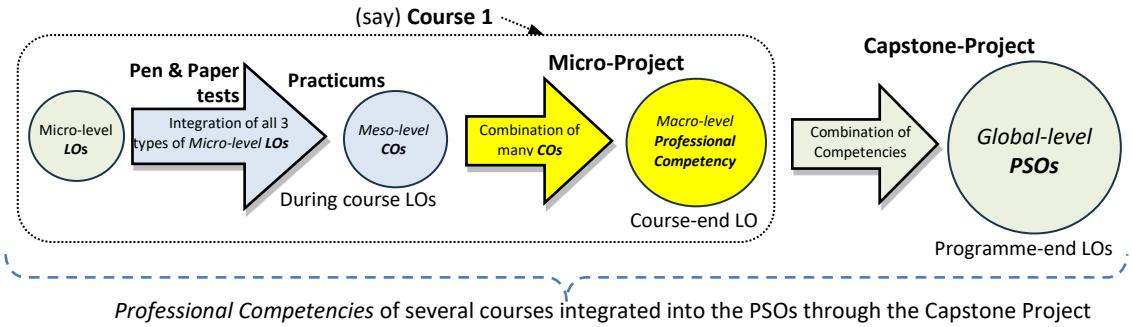


Figure-2. *Distinct Buildup of Micro-level LOs to Global-level LOs through the Semesters*

5.0 Curriculum Development Process of OBCFC "Alliance Model 2025"

At the very outset, this university made a significant gesture of establishing the *Curriculum Development Centre (CDC).* This was crucial to oversee all the curriculum development activities from *Planning the Curriculum* phase to *Evaluating the Curriculum* phase. The CDC then involved the entire teaching fraternity to go through the generic *PDIE Curriculum Development Model* (see figure 3), so that they get equipped in advance for scientifically *Implementing the OBCFC "Alliance Model 2025"* in *letter and spirit*.

Another challenge of OBE in India is the erroneous interpretations of the OBE related terminologies. Due to plethora of interpretations of the OBE related jargons available on various platforms, every university adapted the meaning of the OBE jargons that suited them most. This resulted in the distorted *designs* of OBE curricula leading to their skewed *implementations.* Hence, the authors educated all the concerned, regarding the right interpretations of the various OBE jargons (see Annexure-4).

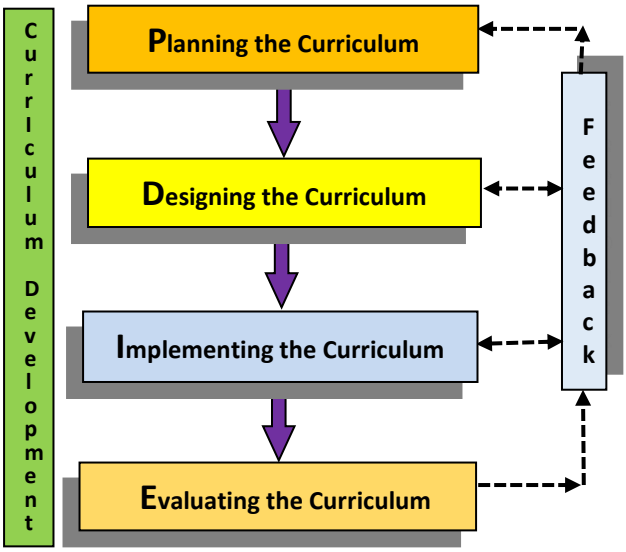


Figure-3. *Generic PDIE Curriculum Development Approach*

A major drawback of the pre-NEP-2020 *traditional syllabi* was the weak industry-connect that lead to high rate of unemployed graduates. Whereas, the post-NEP-2020 OBE curricula require strong industry-connected unambiguously stated LOs in the curriculum in observable and measurable terms (see Annexure-4 and Annexure-5) as adapted in this novel OBE model. This helps all curriculum stakeholders to clearly understand the type of industry-specific LOs to be displayed by the graduates during and at the end of the courses and UG programmes.

5.1 OBCFC "Alliance Model 2025 Programme Structure" Design

It is known that every curriculum has two major parts i.e. the *Programme Structure* and the associated *Course Structures*. Majority of the current so-called OBE *curricula* in HEIs continue to be teacher-centered *Programme Structures* (see Annexure-3) that are not student friendly. Often, the students cannot understand how each course is connected to the jobs that they have to do in the industry. It is often difficult even for the course teacher to decipher the industry expectations from such curriculum. Hence, the authors evolved this *student-friendly* and *industry-aligned "Alliance Model 2025 Programme Structure"* (see Annexure-6).

During *Planning the Curriculum* phase (see figure 3), the concerned teachers were trained to undertake *occupational analysis* of their respective UG programmes to identify the industry needs and governmental requirements, to align with NEP-2020. This process led to the design of opinionnaires to identify the industry-needed macro-level *Professional Competencies* and other types of LOs related to their respective UG programmes (see sample in Annexure-5). These opinionnaires were sent out to respective discipline-specific *industry clusters* for their responses to validate the identified LOs. Their responses to these LOs were statistically analysed and rank-ordered. During *Designing the Curriculum* phase (see figure 3), the rank-ordered *Professional Competencies* were mapped with the related course titles to evolve the OBCFC "*Alliance Model 2025 Programme Structure"* design (see sample in Annexure-6).

This unique innovation of including the macro-level *Professional Competencies* in the *Programme Structure* itself in all the semesters of the UG programmes helps everyone to get a bird's eye-view of the *Competencies* that are to be integrated for developing the UG programme industry-specific *PSOs* (understood as *Goals* by the industry). The parents can now see whether the *Competencies* are for wage-employment, self-employment or for research, before they decide to admit their ward for that particular UG programme. Moreover, at the international level, this novel *Programme Structure* design helps the concerned university, to scrutinise whether the courses with their credits are equivalent for "credits transfer" in admitting the graduates for further studies.

Another feature for rendering the Programme Structure *"student friendly* and *industry-aligned"* is by incorporating the *multi-entry multi-exit (ME-ME)* scheme evidenced in the last line of the "*Note"* in the *Programme Structure* (see Annexure-6). Still another feature is the inclusion of the *educational qualification levels* in each semester [7] as required in NEP-2020 evidenced in the first row of the *Programme Structure* table (see Annexure-6).

5.2 OBCFC "Alliance Model 2025 Course Structure" Design

After the *Programme Structure* was finalised by the CDC, the OBCFC "*Alliance Model 2025 Course Structure"* was designed during the *Designing the Curriculum* phase (see figure 3). This was then followed by designing the second semester *Course Structures* (see Annexure-7), the main foundation stone of the OBE curriculum. Currently, the designing of the third semester *Course Structures* of each UG programme in the Alliance University is going on under the guidance and supervision of the authors.

a) Pre-NEP-2020 and Post-NEP-2020 Course Structures

As discussed earlier in Section-2, the pre-NEP-2020 *traditional syllabi* (see Annexure-2) were *teacher-centered*. Sadly, post-NEP-2020 curriculum, the *teacher-centered* syllabi style still continues (see Annexure-3). The micro-level LOs required to build up the meso-level *industry-specific COs* are missing in most post-NEP-2020 syllabi. Even the macro-level

Professional Competency [4], [6], required by the industry and the accreditation agencies is absent. Most of the post-NEP-2020 courses of the current UG programmes continue to be taught in the old traditional style, whereby the students get only a broad understanding of the topics without knowing the industry-connect. Such syllabi leave the students clueless as to what depth and breadth they have to learn the stated topics to be industry-ready.

In the entire spectrum of the different types of LOs (see figure 2) of a post-NEP-2020 OBE curriculum, the industry is mainly interested in the *macro-level Professional Competency* of each course and the *global-level* Goals/PSOs of a UG programme to be possessed by the graduates. The challenge to develop these and other LOs successfully in the design of *OBCFC* "*Alliance Model 2025 Course Structure"* (see Annexure-7) are discussed in the following sections. This was design was necessary to prepare the students to be industry-ready and also fulfill the *National Guideline Documents'* requirements [4], [5], [7], [8], [9].

b) Significant Features of OBCFC "Alliance Model 2025 Course Structure"

A significant feature of the of this novel design (see Annexure-7) is the "*stem***"** (highlighted in yellow) stated at the beginning of various *Sections* of the *Course Structure*. The *stem* in each section help, especially the new students, to understand the need of the concerned section even without the teacher's explanation. It motivates the students to acquire these LOs through self-learning using the vast information available on various platforms, rendering the *Course Structure student-friendly* and *industry-aligned*.

Section I i.e. "rationale" (see Annexure-7) of the *Course Structure*, provides an overview and informs the student in which industries the LOs of the course will be used. The ultimate aim of the *Course Structure* (see Section II, Annexure-7) is to develop the industry-validated macro-level *Professional Competency* in the student to be industry-ready. Hence, it is the very foundation of this Course Structure. It can be noted that this macro-level competency begins with an observable and measurable action-verb of terminal nature. If this *macro-level LO* is wrongly formulated, all the other dependent *meso-level* and *micro-level* LOs that emerge from the competency will also be flawed, rendering the T-L and assessment efforts of the *teacher and the taught* to be skewed and out-of-place. Such situations can take the *Course Structures* into a tailspin which will be disastrous for the student's future career/livelihood.

Generally, a *macro-level Professional Competency* will have about 4 to 6 *meso-level* sub-tasks emerging from it and termed as *Course Outcomes (COs)* by the academia (see Section III in Annexure-7). Each *meso-level* CO also begins with a single observable and measurable action-verb of terminal nature. Each industry-specific CO is a sub-task that integrates several *micro-level LOs* i.e. Practical Outcomes (PrOs), Attitudinal Outcomes/ Social skills and Intellectual Outcomes associated respectively with the Psychomotor, Affective and Cognitive domains of human learning. Section IV of this model (see Annexure-7) is taken from the 4th row from the table of the *Alliance Model 2025 Programme Structure* (see Annexure-6) to reiterate to the student about the T-L and assessment schemes of this *"Digital Logic Design With VHDL"* course. Every *micro-level LO* also begins with a single observable and measurable action-verb of terminal nature (see Section V, VII, VIII in Annexure-7).

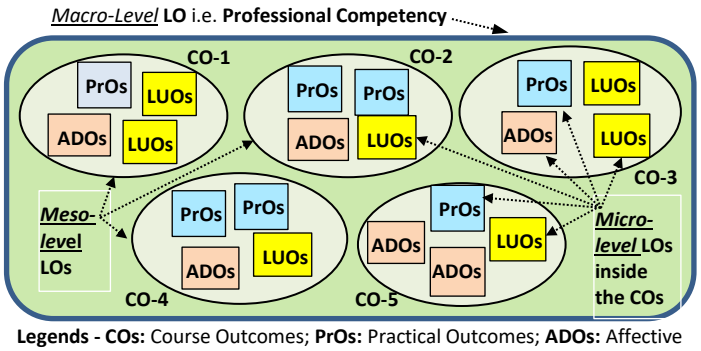
The *micro-level Practical Outcomes (PrOs)* mentioned in the 2nd column (see Section V in Annexure-7) are also the industry-specific skills embedded in the concerned CO. Every PrO and starts with single action verb of terminal nature. The industry requires that each PrO is developed at least to the *D3* expertise level of *Dave's Psychomotor Domain* taxonomy of human learning [13], [15]. To develop each PrO and the industry-related practical skills

associated with it, innovative *Practicum Manuals* have been designed (the scope of which is beyond this paper, but could be discussed at the conference). Section VI in Annexure-7 lists the major resources required to implement each of the PrOs.

An important feature that was not seen in the pre-NEP-2020 traditional syllabi and even now missing in most post-NEP-2020 curricula, but acutely needed by the industry, are the *micro-level LOs* related to the attitudes/social skills i.e. Affective Domain Outcomes (ADOs). Although relatively few, these industry-specific ADOs are an essential part of the *CO i.e* sub-task of the Competency, and hence incorporated in this *Alliance Model 2025* (see Section VII in Annexure-7). Being few, these ADOs are to be repeated multiple times through the various practicums and micro-project to accelerate their development. Every time the ADOs are repeated, they are also assessed with relevant rubrics. This is to happen in every course through the 4 years of every UG programme. Thus, there is ample possibility that by the end of the 4th year, some ADOs are likely to reach the 5th (*K5* level) i.e. *Characterising* [13], [15] level of Krathwohl's taxonomy, thereby fulfilling the industry expectation.

c) Outcome-based Teaching Learning (OBTL)

The inertia to adopt the right OBE philosophy by many universities continues to be the hurdle for the successful implementation of OBE in India. In pre-NEP-2020 curricula, the focus was on teaching the theoretical concepts (see Annexure-1) and often rote-learned by the students. However, in most post-NEP-2020 curricula the T-L transaction continues to maintains the traditional style as the cues for *OBTL* are missing (see Annexure-2). This lacuna is addressed in *Alliance Model 2025*. Due to the unambiguously stated industry-specific LOs (see Section VIII in Annexure-7) in this model and the micro-projects (see Section X), the students get motivated for *self-learning*, a skill acutely required for life-long learning. The *Learning Unit* title is in the 1st column of the 1st row and CO-1 (say) is repeated in the 2nd column, so that the students realize that the micro-level LOs such as industry-specific *Practical Outcomes* (*PrOs)* and the related industry-specific *learning unit outcomes (LUOs)* emerge out from the related CO (see figure 4). Hence, cluster of *PrOs* and *LUOs* are formulated in same 2nd column just below the related CO.



Legends - COs: Course Outcomes; **PrOs:** Practical Outcomes; **ADOs:** Affective Domain Outcomes; **LUOs:** Learning Unit Outcomes of Cognitive Domain

Figure-4. *Micro-level LOs within each Meso-level CO, in a Macro-level LO i.e. Professional Competency*

The LUOs in 2nd column serve as underpinning props for developing the PrOs as well. The focus of the LUOs is on developing *higher order thinking skills* (HOTS) of the Cognitive Domain i.e. '*Apply'* and above levels of Revised Bloom's Taxonomy (RBT), thereby establishing the industry-connect [13], [15]. From meso-level and micro-level LOs in 2nd column, the topics and sub-topics emerge out into 3rd column (see Section VIII Annexure-7). Thus, the PrOs and LUOs in 2nd column and the topics in the 3rd column provide sufficient cues to the *teacher and the taught* for undertaking *OBTL* and *OBA*.

d) Outcome-based Assessment (OBA)

A glaring issue of the pre-NEP-2020 *traditional syllabi* (see Annexure-1) was absence of assessment strategies. Even now, it is not seen in most post-NEP-2020 curricula (see

Annexure-2). Hence, the teachers are often at a loss, as to how to implement *"Outcome-Based Assessment (OBA)"* effectively. The most significant feature of OBA is that, the teachers are required to assess the attainment of the *'Apply'* and above-level RBT related LUOs of the 2nd column (see section VIII Annexure-7) as the understanding of the *concepts* and *principles* get naturally evidenced when the LUOs and the PrOs are exhibited by the students in the examinations. Currently, most of the questions in the examinations assess only the *Remember* and *Understand* levels LOs of RBT [8]. This issue has been addressed in this *Model* by incorporating the "***Table of Specifications (TOS)"*** (see Section IX, Annexure-7)**.** The *TOS* informs the students in advance of how they will be assessed. It serves as a blueprint for the examiner for the design of the pen-and-paper (and even online) question paper for continuous and summative assessment of the attainment of the LUOs. *TOS* also guides examiners to design new *valid* and *reliable* questions year-after-year without any ambiguity and repetition in the examinations.

The attainment of the PrOs and the ADOs are also continuously assessed using custom-designed OBCFC Practicum Manuals (the scope of which is beyond this paper, but could be discussed at the conference). Each practicum is assessed for the attainment of the industry needed pre-determined *process-related skills* and *product related skills* using relevant assessment tools and rubrics, *during* and *after* the conduction of each practicum.

e) Micro-Projects for Assessing the Attainment of Professional Competency and COs

Ultimately, the industry is interested in the *Professional Competency* and the *sub-tasks (i.e. COs)* required to do the related jobs that often come as *projects.* All projects are integration of micro-level LOs and meso-level COs. In OBE, the meso-level COs are deemed to be attained, if the student is able to successfully integrate the related cluster of micro-level LOs in the three domains of human learning for doing various jobs Hence, every OBE *Course Structure* needs to provide opportunities for integrating and combining the micro-level LOs and COs, and the "*micro-project"* (see Section X in Annexure-7) an effective strategy has been adapted in this OBCFC *Alliance Model of 2025*. It is a totally a group-based student-centered strategy where the students undertake the micro-project beyond the contact hours. As it is a group-based strategy, the relatively weak students in each group are likely to get *pulled-up* academically by the stronger students due to the team working. It also inculcates the habit of *self-learning* in the students and even encouraging them to take up complex micro-challenges. It is administered and assessed progressively through every semester using custom-designed *rubrics* for ensuring the integration of the different types of micro-level LOs into the meso-level COs and macro-level Professional Competency (see figure 4). The remaining OBCFC *Course Structure* sections in Annexure-7 are self-explanatory.

6.0 Summary

The uniqueness of this paper is the evolution of the novel *OBCFC "Alliance Model 2025"* consisting of the OBCFC *Programme Structure* and *Course Structure* designs within it, which is a requirement of NEP-2020 required "*Competency-based Framework*". The examples in the annexures provide greater clarity of this novel OBE curriculum model. The distinct buildup of the *micro-level **LOs*** i.e. PrOs, ADOs, LUOs" (see figure 2) to the *macro-level **LO*** i.e. Professional Competencies of every course, and the *Global-level* PSOs of the UG programme (see Annexure-6 and Annexure-7) is well discussed in this paper. The combination of the different types of *meso-level* COs in the *micro-projects* (see Section X in Annexure-7) motivates self-learning in the students to enhance their employability levels. Annexure-8 is the summarised takeaway of the significant features of this innovative model.

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Annexure-1

Traditional UG Syllabus Pre-NEP-2020 Sample

B. Tech. in Electrical Engineering
First Semester

Course Code:	'xyz'	**Credits**			
		L	**T**	**P**	**Total**
Course Title:	**Computer Organization and Architecture**	3	0	1	4

Module No. & Title	**Teaching Hours**	**Topics and Sub-Topics**
Module: I Computer Architecture	**15**	Computer architecture concepts – Register and Stack Organization – Instruction Set Architecture (ISA) – Addressing Modes – Interrupt Cycles – RISC and CISC architecture
Module: II Processor Design	**15**	Arithmetic and Logic Unit – Arithmetic operations – Logical Operations – Control Unit – Hardwired control unit – Micro programmed control unit – Pipelining and Hazards
Module: III Memory Organization	**15**	Primary Memory and Secondary Memory – Memory Hierarchy – Solid-State Drive (SSD) – Stack and Heap – Cache Memory – Cache Mapping Techniques – Direct Memory Access (DMA)
Module: IV I/O Interfacing	**15**	Programmable Peripheral Interface – LCD and LED Interface – Keypad Interface, Analog-to-Digital Converter – Digital-to-Analog Converter – Universal Serial Bus (USB)
Module: V Emerging AI Processor Architecture	**15**	AI Accelerators – Graphic Processing Unit (GPU) – NVIDIA L4 Tensor Core GPU Architecture – Field Programmable Gate Array (FPGA) – Tensor Processing Unit (TPU) – Neural Processing Unit (NPU) – Vision Processing Unit (VPU)

Suggested Books

Title of Book	**Author**	**Publication Details**
Computer Organization and Architecture:Designing for Performance.	William Stallings	Pearson Education, 11th Edition (2019).
Microprocessor Architecture Programming and Application	Ramesh S. Gaonkar	Penram International, Mumbai, 6th Edition
Artificial Intelligence Hardware Design: Challenges and Solutions	Albert Chun-Chen Liu, Oscar Ming Kin Law	John Wiley & Sons (2021),

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Annexure-2

Non-example of Current OBE UG Course Curriculum Post-NEP-2020

B. Tech. in Electrical Engineering
First Semester

Course Code:	'xyz'	**Credits**			
		L	**T**	**P**	**Total**
Course Title:	**Computer Organization and Architecture**	3	0	1	4

Course Outcome -1: ***Understand*** the system functionality of a computer architecture.
Course Outcome -2: ***Analyse*** the performance of the processor functionalities.
Course Outcome -3: ***Explain*** memory functions and techniques influencing performance.
Course Outcome - 4: ***Understand*** interfacing techniques for enhancing the input-output operations.
Course Outcome -5: ***Discuss*** AI architecture for high-end processing applications.

Module No. & Title	**Teaching Hours**	**Topics and Sub-Topics**
Module: I Computer Architecture	**15**	Computer architecture concepts – Register and Stack Organization – Instruction Set Architecture (ISA) – Addressing Modes – Interrupt Cycles – RISC and CISC architecture

Course Code:	'xyz'		Credits			
			L	T	P	Total
Course Title:	Computer Organization and Architecture		3	0	1	4
Module: II Processor Design	**15**	Arithmetic and Logic Unit – Arithmetic operations – Logical Operations – Control Unit – Hardwired control unit – Micro programmed control unit – Pipelining and Hazards				
Module: III Memory Organization	**15**	Primary Memory and Secondary Memory – Memory Hierarchy – Solid-State Drive (SSD) – Stack and Heap – Cache Memory – Cache Mapping Techniques – Direct Memory Access (DMA)				
Module: IV I/O Interfacing	**15**	Programmable Peripheral Interface – LCD and LED Interface – Keypad Interface, Analog-to-Digital Converter – Digital-to-Analog Converter – Universal Serial Bus (USB)				
Module: V Emerging AI Processor Architecture	**15**	AI Accelerators – Graphic Processing Unit (GPU) – NVIDIA L4 Tensor Core GPU Architecture – Field Programmable Gate Array (FPGA) – Tensor Processing Unit (TPU) – Neural Processing Unit (NPU) – Vision Processing Unit (VPU)				

Suggested Books

Title of Book	Author	Publication Details
Computer Organization and Architecture:Designing for Performance.	William Stallings	Pearson Education, 11th Edition (2019). ISBN: 978-0-13-499719-3
Microprocessor Architecture Programming and Application	Ramesh S. Gaonkar	Penram International, Mumbai, 6th Edition (2013)
Artificial Intelligence Hardware Design: Challenges and Solutions	Albert Chun-Chen Liu, Oscar Ming Kin Law	John Wiley & Sons (2021),

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Annexure-3

A non-example of UG Current Programme Structure Post-NEP-2020

B. Tech. in Electrical Engineering
First Semester

Sr. No.	Course Type	Course Code	Course Name	L	T	P	S	Cr	Evaluation Scheme (Weightages in %)				
									Theory			Laboratory	
									MSE	TA	ESE	ISE	ESE
01	BSC	<*tbd*>	Matrix Algebra, Calculus and Probability	2	1	0	1	3	30	10	60	--	--
02	BSC	<*tbd*>	Engineering Chemistry	2	0	2	1	3	30	20	50	CIE: 100	
03	BSC	<*tbd*>	Biology for Engineers	2	0	0	1	2	30	20	50	--	--
04	ESC	<*tbd*>	Elements of Electronics Engineering	2	0	2	1	3	30	20	50	CIE: 100	
05	ESC	<*tbd*>	Engineering Mechanics	2	0	2	1	3	30	20	50	CIE: 100	
06	ESC	<*tbd*>	Programming for problem solving	2	0	2	2	3	30	20	50	CIE: 100	
07	IKS	<*tbd*>	Indian Knowledge System	2	0	0	1	2	CIE: 100			--	--
08	CCA	<*tbd*>	Liberal Learning course - I	0	0	2	0	1	--	--	--	CIE: 100	
Total				**14**	**01**	**10**	**10**	**20**					

Legends: **L**-Lecture, **T**-Tutorial, **P**-Practical, **S**-Self Study, **Cr**-Credits **ISE**-In-Semester-Evaluation, **ESE**-End-Semester-Evaluation , **MSE**-Mid-Semester-Evaluation, **TA**-Teachers' Assessment, **CIE**-Continuous-Internal-Evaluation

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Annexure-4

Definitions of OBE Terms in OBCFC "Alliance Model 2025"

These are the definitions that are according to the National Guideline Documents and also universally understood and widely accepted across the world. Hence, they have been adapted in the *"Alliance Model 2025"*.

Learning Outcome (LO): Every ***LO*** is known for its fundamental two characteristics i.e. 'measurability' and 'observability'. Such LOs in a course and program can range from micro-level LOs such as the Practical Outcomes (PrOs), to Global level LOs such the Program Specific Outcomes (PSOs). Absence of these two characteristics does not qualify any statement to be a LO.

Program Educational Objective (PEO): The '***Aim***' of any curriculum as understood by the industry is the futuristic industry-specific ***'PEO'*** stated at a '*Universal level*'. It describes the expertise the graduate would be able to display after 4-6 years of working in the industry due to the concerned program. The PEOs are validated by the industry in tune with government regulations (see figure 'a').

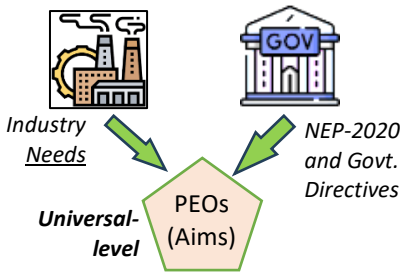


Figure 'a': Universal-level PEOs

Program Specific Outcome (PSO): The *'Global level'* industry-specific ***'PSO'*** is a LO of an occupation that is understood by the industry as the '*Goal*' of any curriculum and required to be displayed by the graduate by graduation day. It is also validated by the industry in tune with government regulations (see figure 'b').

Professional Competency: Unlike, 'PEOs' and 'PSOs', the '*Macro level*' job-specific term ***'Professional Competency'*** of an occupation is well understood, equally by the academia and the industry alike. It is the '*foundation stone*' of each OBE *'Course'* curriculum to align with the Government of India promulgated OBE *'Competency-based Framework'*. It is also validated with the industry-related main task (see figure 'c'). This *Professional Competency* in a particular occupation is defined '*as a statement that indicates the successful completion of a macro-level main task at the threshold level without hurting oneself, wasting raw materials, damaging any device and beginning with a SMART action verb of terminal nature consisting of a cluster of sub-tasks/skill-sets'* and is generally related to a particular "course" of a UG/PG program.

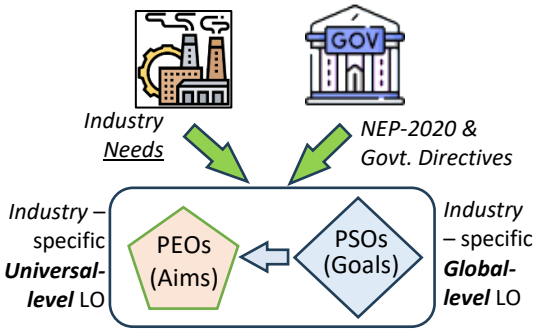
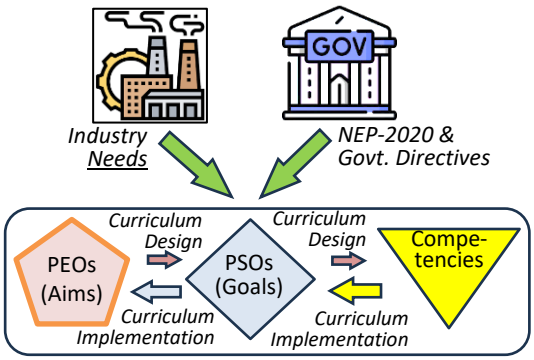


Figure 'b': Global-level PSOs

Course Outcome (CO): The CO is an industry-specific *Meso-level* 'sub-task' (see figure 'd') of the main task i.e. '*Professional Competency*'. Typically, a 4-credit course in a UG program consists of 5 to 6 COs co-related to 5 to 6 'learning units' including topic clusters.

Course: A *'Course'* is a knowledge chunk that emerges out from the related '*body of knowledge (also called subject)*', which can be reasonably transacted in the institutional classrooms/laboratories/ workshops and online mode. A *'Course'* such as 'Basic Physics', 'Artificial Intelligence', 'Machine Learning' and so on, is defined as "*a collection of meso-level COs and other micro-level LOs, such as the Practical Outcomes, Attitudinal Outcomes and Intellectual Outcomes, related topics"* to be learned by the students as they sail through each semester.



Figure'c': Macro-Level Professional Competencies

Practicum: The practicums are hands-on-learning activities undertaken to develop the Practical Outcomes and also the Attitudinal Outcomes, generally outside the four walls of the classroom in the laboratories/workshops/ fields and so on, as needed at the workplace/industry.

Credit/Academic Credit: It is a universally accepted measuring unit to measure the academic coursework. A 1-credit indicates 1-hour of lecture (classroom)/tutorial session with the instructor every week for a total of 15 hours in a semester. Whereas, a 1-credit 'Practicum' means 2-hours of active engagement every week in the laboratory/workshop/seminar/studio/field resulting in a total of 30 hours in a semester.

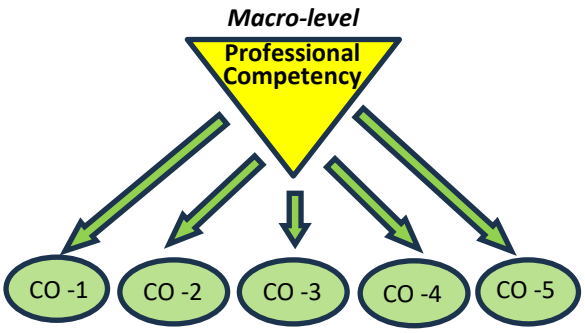


Figure 'd': Meso-level Industry-specific *COs*

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Annexure-5

Opinionnaire of Learning Outcomes Required by Industry

S. No.	**Professional Competencies** (at Entry Level) (i.e. Macro-level ***jobs*** required ***entry level*** that a B.Tech. graduate must ***DO*** in order to justify his/her salary in your industry) **Legends**: ***ME:*** *Most essential;* ***E:****Essential;* ***D:****Desirable;* ***RN:*** *Rarely Needed*	Tick (√) in any one cel			
		ME	**E**	**D**	**RN**
	Generic Competencies Required in this Occupation				
G-1	***Communicate*** effectively in English in oral and written form.				
G-2	***Develop*** engineering drawings manually and with relevant computer software.				
G-3	***Use*** principles of Physics to solve the problems in Electrical and Electronics engineering.				
G-4	……and so on				
	Core Professional Competencies Required in this Occupation				
C-1	***Use*** different types of tools and measuring instruments to troubleshoot various kinds of electrical and electronic circuits.				
C-2	***Evaluate*** the choice of electrical engineering materials used in various applications.				
C-3	……and so on				

S. No.	**Goals of this Curriculum** [known as Programme Specific Outcomes (PSOs) by Academia] (i.e. Global level jobs that a B.Tech. Engineer has to ***DO*** at the ***entry level*** to the industry) **Legends: SA:** Strongly Agree, **A:** Agree, **D:** Disagree, **SD:** Strongly Disagree	Tick (√) in any one cell			
		SA	**A**	**D**	**SD**
P-1	***Evaluate*** the performance of electric drives and control systems.				
P-2	……and so on				
P-3					

S. No.	**Aims of this Curriculum** [known as Programme Educational Objectives (PEOs) by Academia] (i.e. Expertise areas at the Universal level that a B.Tech. Engineer would have acquired after having worked in your industry for 4 to 6 years) **Legends: SA:** Strongly Agree, **A:** Agree, **D:** Disagree, **SD:** Strongly Disagree	Tick (√) in any one cell			
		SA	**A**	**D**	**SD**
A-1	***Enhance*** the performance of microgrids in renewable energy system.				
A-2	……and so on				
A-3					

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Annexure-6

OBCFC "Alliance Model 2025"

UG Programme in Electronics and Communication Engineering

Student-Friendly and Industry-Aligned
OBCFC Programme Structure
[Choice-based Multi-Entry and Multi-Exit (ME–ME)]

I -Semester

Semester: I – Electronics and Communication Engineering												**Level-4.5 UG Certificate**		
S. No.	**Course Code**	**Course Category**	**Competency** (Entry level Macro-level Job that a Graduate has to DO in Industry)	**Course Title**	**Teaching-Learning Scheme** Hours/semester (**Credits**)						**Examination Scheme** (Marks)		
					L Hrs/ sem ***Credits***	**T** Hrs/ sem ***Credits***	**P** Hrs/ sem ***Credits***	**TW** (Hrs/semester) **SL** Hrs/ sem	**MP** (Hrs/sem) for CO development by SL)	Total Hrs/30 = ***Credits***	**CIE** (**L**UO+Pr O+ADO) ***(Qualifying marks)***	**SEE** (LUO+Pr O) ***(Qualifying marks)***	**Total Marks** ***(Qualifying marks)***
1	Z5AML25201	BSC	***Use*** the principles of multi-variable calculus and differential equations for solving various problems in Electrical and Electronics engineering.	Multivariable Calculus and Differential Equations	30 **(2)**	15 **(1)**	30 **(1)**	25	20	120/ 30 = ***4***	60 ***(30)***	40 ***(20)***	100 ***(50)***
2	Z5SCB25200	BSC	***Use*** the principles of chemistry for solving complex engineering problems.	Basic Chemistry	30 **(2)**	15 **(1)**	30 **(1)**	25	20	120/ 30 = ***4***	60 ***(30)***	40 ***(20)***	100 ***(50)***
3	E2ECA25200	UCC	***Innovate*** simple engineering models to fulfil user needs using cross-disciplinary knowledge.	Innovations and Inventions in Engineering	15 **(1)**	0	30 **(1)**	15	0	60/ 30 = ***2***	60 ***(30)***	40 ***(20)***	100 ***(50)***
4	Z5SCA25201	BSC	***Use*** the principles of Physics for solving problems related to electrical and electronics engineering.	Physics-I	30 **(2)**	15 **(1)**	30 **(1)**	25	20	120/ 30 = ***4***	60 ***(30)***	40 ***(20)***	100 ***(50)***
5	E1CSA25201	AEC	***Develop*** modular Java programs for solving various problems with logical reasons.	Logic Building using JAVA	15 **(1)**	0	30 **(1)**	0	15	60/ 30 = ***2***	60 ***(30)***	40 ***(20)***	100 ***(50)***
6	Z5SCA25203	BSC	***Solve*** healthcare problems using the principles of biological and biomedical engineering.	Biology	30 **(2)**	0	30 **(1)**	10	20	90/30 = ***3***	60 ***(30)***	40 ***(20)***	100 ***(50)***
7	L1PPA25200	VAC	***Prepare*** project proposals for different requirements incorporating the Sustainable Development Goals (SDGs).	Sustainable Development Goals	15 ***(1)***	0	0	5	10	30/30 = ***1***	50 ***(25)***	0	50 ***(25)***
8	A1PHR25107	AEC	***Adapt*** relevant learning techniques to acquire the various types of learning outcomes	Learning How to Learn	0	0	0	15	0	0	0	0	0
9	A1PHR25108	AEC	***Generate*** effective prompts for optimizing responses in various applications using AI language models.	Prompt Engineering	0	0	0	36	0	0	0	0	0
10	A1PHR25109	VAC	***Prepare*** personalized academic development plans for career aspirations	Advising Seminar	0	0	0	0	0	0	0	0	0

Semester: I – Electronics and Communication Engineering												Level-4.5 UG Certificate		
S. No.	Course Code	Course Category	Competency (Entry level Macro-level Job that a Graduate has to DO in Industry)	Course Title	Teaching-Learning Scheme Hours/semester (Credits)						Examination Scheme (Marks)		
					L Hrs/ sem Credits	T Hrs/ sem Credits	P Hrs/ sem Credits	TW (Hrs/semester) SL Hrs/ sem	TW (Hrs/semester) MP (Hrs/sem) for CO development by SL)	Total Hrs/30 = Credits	CIE (LUO+PrO+ADO) (Qualifying marks)	SEE (LUO+PrO) (Qualifying marks)	Total Marks (Qualifying marks)
11	A1PHR25101	LBC	***Demonstrate*** involvement in co-curricular and extra-curricular activities for building leadership, collaboration, and social responsibility skills.	Activity Points 1	0	0	0	0	0	100 Pts	0	0	0
				Total	**11**	**3**	**6**	**171**	**0**	**20**			

Legends

L: *Lecture;* ***T:*** *Tutorial;* ***P:*** *Practicum;* ***TW****: Term-Work;* ***SL****: Self-Learning;* ***MP****: Micro-Project;* ***PrOs:*** *Practical Outcomes;* ***LUOs:*** *Learning Unit Outcomes;* ***ADOs:*** *Affective Domain Outcomes;* ***CIE:*** *Continuous Internal Examination;* ***SEE****: Semester-End-Examination;* ***AEC****: Ability Enhancement Course;* ***BSC****: Basic Science Course;* ***ESC:*** *Engineering Science Course;* ***PCC****: Programme Core Course;* ***VAC:*** *Value Added Course;* ***UCC:*** *Engineering Core Course:* ***LBC:*** *Learning Beyond Classroom;* ***Pts****:Points*

Note: Out of ***60 marks for CIE***, **10** marks each for **2** tests for LUO assessment; **15** marks for Practicum assessment; **20** marks for ***Micro-project*****;** **5** marks for class notes. The ***Rubric*** of the ***Micro-project*** assesses the integration of the COs for the attainment of the ***Professional Competency***. ***If any student wants to exit with certification, under multi-entry multi-exit (ME-ME) scheme, the student will have to qualify all the courses up to the second semester and additionally s/he has also to qualify 2 Skill Enhancement Courses (SECs) of 4 credits each during the summer break.***

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Annexure-7

OBCFC "Alliance Model 2025"

UG Programme in in Electronics and Communication Engineering

Student-Friendly and Industry-Aligned
OBCFC Course Structure
[Choice-based Multi-Entry and Multi-Exit (ME–ME)]

Course Code: **……**
Course Title: **Digital Logic Design With VHDL**

PEO-1: ***Improve*** wireless and cellular networks, addressing complex challenges for ensuring reliable communication. (Universal level)

PSO-1. ***Integrate*** the hardware and software co-designs for Embedded systems and IoT applications to achieve optimal performance *(Global level LO)*
PSO-2. ***Optimize*** next generation communication systems. *(Global level LO)*
PSO-3. ***Evaluate*** the VLSI circuits and systems, to ensure optimal performance. *(Global level LO)*

UG Programme	Course Category	Pre-requisite Course	Semester
ECE	PCC	-	Third

I. RATIONALE

The outcomes of this course are used in feedback circuits such as aerospace, automotive, healthcare, renewable energy power plants, power systems and so on. Furthermore, understanding the interaction between analog and digital domains is vital for designing mixed-signal systems that dominate today's technological landscape. Such knowledge is essential in understanding the function of electronic components, circuit analysis, and system design. It fosters critical thinking and problem-solving skills by introducing key concepts such as amplification, filtering, Boolean logic, logic gates, flip-flops, counters, and digital circuit design techniques.

II. PROFESSIONAL COMPETENCY

The basic purpose of this one sentence, is to help the student to develop the following macro-level professional competency, which is an entry-level industry-specific main task that is to be attained by the student through this course and its attainment assessed through the micro-project**:**

- ***Evaluate*** *the performance of digital logic circuits with VHDL in various engineering applications.*

III. COURSE OUTCOMES (COs)

Each of the following course outcomes (COs) are ***industry-specific*** *meso-level* ***sub-tasks*** of the above-referred ***professional competency*** and its attainment assessed through the ***micro-project:***

CO-1. ***Evaluate*** the use of number systems and minimization techniques of digital circuit designs.
CO-2. ***Develop*** VHDL designs of various digital systems.
CO-3. ***Evaluate*** performance of digital combinational circuits.
CO-4. ***Evaluate*** performance of digital sequential circuits.
CO-5. ***Evaluate*** the designs of the counters and Finite State Machines.

Undertaking the ***micro-project*** related to the above-referred industry-specific '*competency'* (i.e. main task) of this course, enables the ***integration*** of the above-mentioned industry-specific COs (i.e. sub-tasks). The micro-project also provides '*experiential learning',* as it simulates the work-place/industry environment as the student group undertakes the micro-project through the semester working at least one hour every week. Thereby, the micro-project also assesses the attainment of the COs and the competency ultimately required by the industry.

IV. TEACHING AND EXAMINATION SCHEME

Teaching and Learning Scheme						**Examination Scheme** (Marks)		
L Hrs./sem. ***(Credits)***	**T** Hrs./sem. ***(Credits)***	**P** Hrs/sem ***(Credits)***	**TW** (Hrs./sem.) **SL** (Hrs./sem. of web-based course)	**TW** (Hrs./sem.) **MP** (Hrs/sem. for CO development by SL)	Total Hrs./30 = **Credits**	**CIE** = LUOs+(PrOs+ADOs) +MP + Class notes ***(Qualifying marks)***	**SEE** (for LUOs) ***(Qualifying marks)***	**Total Marks** ***(Qualifying marks)***
30 ***(2)***	15 ***(1)***	30 ***(1)***	25	20	120/30 = ***4***	60 = (10+10+15+20+5) ***(30)***	40 ***(20)***	100 ***(50)***

Legends: ***L:*** *Lecture;* ***T:*** *Tutorial;* ***P:*** *Practicum;* ***TW****: Term-Work;* ***SL****: Self-Learning;* ***MP****: Micro-Project;* ***PrOs****: Practical Outcomes;* ***LUOs:*** *Learning Unit Outcomes;* ***ADOs:*** *Affective Domain Outcomes;* ***CIE:*** *Continuous-Internal-Examinations;* ***SEE****:Semester-End-Examination.*

Note: Out of ***60 marks for CIE***, **10** marks each for **2** tests for LUO assessment; **15** marks for Practicum assessment; **20** marks for ***Micro-project*****; 5** marks for class notes. The ***Rubric*** of the ***Micro-project*** assesses the integration of the COs for the attainment of the ***Professional Competency***.

V. PRACTICUMS

The following are the industry-specific ***micro-level LOs*** i.e. *practical outcomes* (PrOs) or *practicum statements* that emerge out from the *COs* and *competency.* These are to be acquired by the UG students, to the 3rd level (i.e. *D3 'Precision'* level) of ***Dave's Psychomotor Domain taxonomy*** of human learning. The best places where PrOs can be developed are the laboratories/workshops/field or micro-projects.

Note: Assessment of PrOs are based on the attainment of the Process (P) and Product (P) related LOs/skills

PrO. No.	**Related CO**	**Practicum Statement (Micro-level Practical Outcome)**	Hours Required / **Dave's Taxonomy**	**Assessment in each Practicum**
1	CO-1	***Design*** *a code converter for* ***the given*** *application.*	02 / **D3**	P and P
2	CO-2	***Evolve*** *a VHDL code for* ***the given*** *digital logic circuit.*	02 / **D3**	P and P
3	CO-2	***Design*** *a digital logic circuit for* ***the given code conversion*** *using VHDL*	02 / **D3**	P and P
4	CO-3	***Design*** ***the given*** *Adder/ Subtractor digital logic circuit using* ***the specified*** *VHDL behavioural architecture code.*	02 / **D3**	P and P
5	CO-3	***Design*** ***the given*** *adder/subtractor digital logic circuit using digital ICs.*	02 / **D3**	P and P
6	CO-3	***Design*** *a digital logic circuit for* ***the given*** *magnitude comparator.*	02 / **D3**	P and P
7	CO-3	***Design*** *a digital logic circuit for* ***the given*** *generator and checker*	02 / **D3**	P and P
8	CO-3	***Test*** *the performance of* ***the given*** *MUX \ DEMUX using VHDL programming.*	02 / **D3**	P and P
9	CO-3	***Test*** *the performance of* ***the given*** *MUX/ DEMUX using IC 74153 / IC 74139*	02 / **D3**	P and P
10	CO-4	***Evaluate*** *the functionality of* ***the given*** *Flip Flops.*	02 / **D3**	P and P
11	CO-4	***Test*** *the performance of* ***the given*** *7-segment static display system for displaying the numbers 0 to 9*	02 / **D3**	P and P

PrO. No.	Related CO	Practicum Statement (Micro-level Practical Outcome)	Hours Required / Dave's Taxonomy	Assessment in each Practicum
12	CO-5	***Design*** *an Asynchronous counter for* ***the given*** *MOD value.*	02 / **D3**	P and P
13	CO-5	***Design*** *Ring and Jhonson Counter for* ***the given*** *specification*	02 / **D3**	P and P
14	CO-5	***Design*** *an up-down counter for* ***the given*** *count using VHDL programming*	02 / **D3**	P and P
15	CO-5	***Design*** *a shift register for* ***the given*** *expression using VHDL programming.*	02 / **D3**	P and P
		Total	**30 hours**	

VI. RESOURCES REQUIRED

This section prepares the students to learn about the specifications of the equipment and consumables with respect to the PrOs in section V, that they will be required to handle in the workplace/industry.

S. No.	Resource Name	Broad Specifications	Qty	Practicum No.
1	Digital trainer	Table top model with 2 bread boards.	30	1-11
2	NOT gate	IC 7404	30	1-11
3	AND gate	IC7408	30	1-11
4	OR gate	IC7432	30	1-11
5	Ex-OR gate	IC7486	30	1-11
6	NOR gate	IC 7402	30	1-11
7	NAND gate	IC 7400	30	1-11
8	EX-NOR gate	IC 4077	30	1-11
9	MUX	IC74153	30	5
10	DEMUX	IC74139	30	5
11	3 input NAND gate	IC 7410	30	8
12	JK Flip Flop	IC 7476	30	10
13	BCD to 7 Segment Decoder	IC 7447	30	9
14	Seven Segment Display	Common Cathode	30	9
15	Shift Register	IC 7495	30	11

VII. AFFECTIVE DOMAIN OUTCOMES (ADOs)

The following are industry-needed ***micro-level LOs*** or social skill/attitudes related to the *Affective Domain Outcomes (**ADOs**)* of human learning that emerge from the COs and professional competency. The industry needs them acutely and expects the students to acquire them through this and other courses.

1) ***Follow*** safe practices.
2) ***Function*** as a team member.
3) ***Follow*** good house keeping
4) ***Follow*** ethics.

Such ***ADOs*** cut across many courses of the UG programme and industry expects them to be developed at the 5th level of *Krathwohl's* ***(K1*** to ***K5)*** ***'Affective Domain'*** taxonomy (i.e. 'characterizing' level) gradually and the best places are in the laboratories/workshops/field or micro-projects:

a) *'Responding'* level in 1st year (**K2**)
b) *'Valuing'* level in 2nd year (**K3**)
c) *'Organizing'* level in 3rd year (**K4**)
d) '*Characterizing*' level in 4th year (**K5**).

VIII. UNDERPINNING LEARNING UNIT OUTCOMES (LUOs)

The following are the industry-specific ***micro-level LOs*** at the ***'Apply***' and above six levels of ***Revised Bloom's Taxonomy*** (***RBT-1*** to ***RBT-6***). Related to the ***Cognitive Domain,*** these *LOs* termed as *learning unit outcomes* (LUOs) are to be acquired by every student through each course. The LUOs are needed to undertake the PrOs embedded in the *industry-specific COs* and *Professional Competency*.

Note: The green shaded matter is for self-learning (SL)

Learning Unit (LU) No. and Title	Meso-level LOs and Micro-level LOs	Topics and Sub-topics
Unit-I **Number systems and Minimization Techniques**	***CO-1. Evaluate the use of number systems and minimization techniques of digital circuit designs.*** **PrO 1.** ***Design*** *a code converter for* ***the given*** *application.* LUO-1a. ***Interpret*** ***the given*** expression in terms of Minterms and Maxterms. LUO-1b. ***Simplify*** ***the given*** Boolean expression. LUO-1c. ***Design*** a digital logic circuit for ***the given*** application. LUO-1d. ***Design*** a logic circuit for ***the given*** code conversion.	1.1 Number systems. 1.2 Minterms and maxterms expressions 1.3 Algebraic method 1.4 Karnaugh maps with 5 and 6 variables, don't care condition and Quine McCluskey, Minimization Technique. 1.5 Codes: BCD, Gray Excess- 3.
Unit-II **Digital Circuit Design with VHDL**	***CO-2. Develop VHDL designs of various digital systems.*** **PrO 2.** ***Evolve*** *a VHDL code for* ***the given*** *digital logic circuit.* **PrO 3.** ***Design*** *a digital logic circuit for* ***the given code conversion*** *using VHDL* LUO-2a. ***Design*** a combinational circuit for ***the given*** Boolean expression using ***the specified*** modelling style. LUO-2b. ***Design*** *a* counter with ***the specified*** Flip flop using ***the given*** modelling style. LUO-2c. ***Design*** a register with ***the specified*** Flip flops using ***the given*** modelling style. LUO-2d. ***Design*** the memory block for ***the given*** specifications.	2.1. VHDL design flow, program structure, 2.2. Data flow design elements, behavioral design elements 2.3. VHDL design elements - structural design elements. 2.4. Memory functions and procedures, libraries and packages
Unit – III **Combinational circuits**	***CO-3. Evaluate performance of digital combinational circuits.*** **PrO 4.** ***Design*** ***the given*** *Adder/ Subtractor digital logic circuit using* ***the specified*** *VHDL behavioural architecture code.* **PrO 5.** ***Design*** ***the given*** *adder/subtractor digital logic circuit using digital ICs.* **PrO 6.** ***Design*** *a digital logic circuit for* ***the given*** *magnitude comparator.* **PrO 7.** ***Design*** *a digital logic circuit for* ***the given*** *generator and checker.* **PrO 8.** ***Test*** *the performance of* ***the given*** *MUX \ DEMUX using VHDL programming.* **PrO 9.** ***Test*** *the performance of* ***the given*** *MUX/ DEMUX using IC 74153 / IC 74139.* LUO 3a. ***Interpret*** ***the given*** adder and subtractor digital circuit. LUO 3b. ***Interpret*** the comparator circuit for ***the given*** application. LUO 3c. ***Design*** a digital logic circuit using Encoder and Decoder for ***the given*** Boolean expression for ***the specified*** application. LUO 3d. ***Design*** a Parity generator and checker for ***the specified*** application LUO 3e. ***Design*** a digital logic circuit using MUX/ DEMUX for ***the given*** Boolean expression for ***the specified*** application. LUO 3f. ***Design*** a logic circuit using Programmable Logic Design for ***the given*** application.	3.1. Arithmetic circuits: adders and subtractor 3.2. Ripple carry adders and Carry look ahead adders 3.3. Adder cum subtractor, BCD Adder and Subtractor 3.4. Comparator 3.5. Decoder, Encoder, Priority encode 3.6. Parity generator and checker 3.7. MUX/DEMUX and their structures 3.8. Logic using ROM array,

Learning Unit (LU) No. and Title	Meso-level LOs and Micro-level LOs	Topics and Sub-topics
Unit – IV **Sequential circuits**	***CO-4. Evaluate performance of digital sequential circuits.*** **PrO 10.** ***Evaluate*** *the performance of* ***the given*** *Flip Flops.* **PrO 11.** ***Test*** *the performance of* ***the given*** *7-segment static display system for displaying numbers 0 to 9.* LUO-4a. ***Justify*** the choice of sequential circuit for ***the given*** application. LUO-4b. ***Modify*** the working of ***the given*** flip-flop for ***the specified*** requirement in ***the given*** scenario. LUO-4c. ***Modify*** the working of ***the given*** synchronous/ asynchronous circuits for ***the specified*** requirement in ***the given*** scenario. LUO-4d. ***Design*** ***the given*** shift register using ***the specified*** set of flip flops for ***the required*** application. LUO-4e. ***Justify*** the choice of counter for ***the given*** scenario.	4.1 Latches and Flip-Flops, triggering methods 4.2 Flip-Flop conversion, Excitation Table, state diagram and applications. 4.3 Synchronous and asynchronous circuits 4.4 Shift Registers, 4.5 Counters
LU – V **Finite State Machines**	***CO-5. Evaluate the designs of the Counters and Finite State Machines.*** **PrO 12.** ***Design*** *an Asynchronous counter for* ***the given*** *MOD value.* **PrO 13.** ***Design*** *Ring and Jhonson Counter for* ***the given*** *specification.* **PrO 14.** ***Design*** *an up -down counter for* ***the given*** *count using VHDL programming.* **PrO 15.** ***Design*** *a shift register for* ***the given*** *expression using VHDL programming.* LUO-5a. ***Design*** a synchronous sequential counter digital logic circuit for ***the given*** count value. LUO-5b. ***Design*** an asynchronous sequential counter digital logic circuit for ***the given*** count/MOD value. LUO-5c. ***Design*** a counter for ***the given*** count values using ***the specified*** model. LUO-5d. ***Design*** a counter for ***the given*** application using state reduction and state assignment. LUO-5e. ***Interpret*** the hazard that can occur in ***the given*** digital circuit.	5.1 Design of counters using sequential circuit approach 5.2 Analysis and synthesis of Asynchronous sequential circuits 5.3 Finite State Machines: Mealy Basic design steps, Moore types, Basic design steps 5.4 State reduction and state assignment, 5.5 Hazards.

IX. TABLE OF SPECIFICATIONS (TOS) FOR DESIGNING QUESTIONS

This *Table of Specifications* (TOS) is the blueprint for distribution of marks for assessing the attainment of micro-level LUOs in the pen-and-paper tests and examinations. The actual distribution of marks in the test/question paper may slightly vary when fulfilling the attainment of the LUOs.

LU No.	Industry Specific Meso-level COs	T-L Hours	Distribution of Marks for Assessing Attainment of Micro-level LUOs through CIE and SEE						
			R Level	U Level	A Level	An Level	E Level	C Level	Total Marks
I	***Evaluate*** the use of number systems and minimization techniques of digital circuit designs.	8	2	8	4	4	8	0	26
II	***Develop*** VHDL designs of various digital systems.	8	0	8	6	4	8	0	26
III	***Evaluate*** performance of digital combinational circuits.	10	2	2	10	4	8	0	26
IV	***Evaluate*** performance of digital sequential circuits.	9	0	2	6	10	8	0	26

LU No.	Industry Specific Meso-level COs	T-L Hours	Distribution of Marks for Assessing Attainment of Micro-level LUOs through CIE and SEE						
			R Level	U Level	A Level	An Level	E Level	C Level	Total Marks
V	***Evaluate*** the design of the Counters and Finite State Machines.	10	0	2	0	12	12	0	26
Total		**Total**	**45**	**4**	**22**	**26**	**34**	**44**	**130**

Legends: T-L:Teaching-Learning; ***SEE***: Semester-End-Examination; ***CIE:*** Continuous-Internal-Examinations; **R**:Remember; **U:**Understand; **A**:Apply; **An**:Analyse; **E:**Evaluate; **C**:Create of ***Revised Bloom's taxonomy (RBT)***

X. SUGGESTED MICRO-PROJECTS

The attainment of the *micro-level* LOs i.e. ***PrOs, ADOs*** and ***LUOs*** is assessed continuously through the *practicum* and *pen-and-paper* tests respectively. Each *meso-level* industry-specific ***CO*** is an ***integration*** of these *micro-level* LOs. The ***workplace/industry-specific micro-project*** provides opportunities for 'out-of-the-box' thinking in the students to integrate the meso-level COs into the *macro-level professional competency*. It inculcates ***self-learning*** in the student (enshrined in the NEP-2020) to solve *micro-level complex problems*, thereby aligning with the *Washington Accord.* It also helps to stimulate the student creativity that may even lead to *micro-level* '*product designs'*. Although a ***suggestive list*** of micro-projects is given here, each ***student group*** is free to choose their own *workplace/industry-specific micro-project*, with the teacher ensuring that every micro-project ***integrates*** at least ***three*** *or more* ***COs*** and ***15 hours*** of individual learning effort reflected in the ***dated work-diary*** maintained by ***each student.*** A new list of micro-projects will be given every year.

1) ***Design*** a Digital Lock System. (CO1-CO5)
2) ***Design*** a Smart Voting Machine Using Combinational and Sequential Logic. (CO3-CO5)
3) ***Design*** a Real-Time Parking Slot Counter Using Sequential Circuits. (CO3-CO5)
4) ***Design*** a Mini ALU Implementation Using Both Hardware Logic ICs and VHDL. (CO1-CO5)
5) ***Design*** a Code Conversion and Error Detection Unit using Parity Generator/Checker and Gray Code Logic. (CO1-CO5)
6) ***Develop*** a VHDL-Based 7-Segment Display Driver for Numeric and Alphabetic Display. (CO1-CO5)
7) ***Design*** Traffic Light Controller. (CO3-CO5)
8) ***Design*** a Vending Machine Controller. (CO3-CO5)
9) ***Design*** a Synchronous Counter-Based Digital Timer Module. (CO3-CO5)
10) ***Design*** of a Multi-Function Logic System Using MUX/DEMUX. (CO1-CO5)
11) ***Design*** an Automated Boolean Expression Simplifier. (CO1-CO5)
12) ***Design*** a digital calculator. (CO1-CO5)

Within 2 weeks of the start of every semester, each group of 4-6 students submits a ***Micro-Project Proposal*** of 1-2 pages in the commonly provided template. The micro-project could be laboratory/ workshop/internet/software or field-based. The ***dated*** micro-project ***work-diary*** is the evidence of ***15 hours*** of his/her individual contribution (other than the contact-hours) in doing the micro-project and will be used for continuous evaluation. This micro-project is undertaken by every student during the free time at home, hostel, or any other place is to gradually build up the skill and confidence to become problem solver as required by the industry.

Based on the ***Micro-Project Proposal action plan***, each group will submit the ***Micro-Project Report*** of not more than 15 pages towards the end of the semester in the given template, followed by a *seminar presentation*. This will be followed by an oral examination of each student for final assessment. By the end of a 4-year UG program, each student would have built up a ***Micro-Project Portfolio*** of 25-30 ***Micro-Project Reports*** - a proud asset that every student can showcase during job-interviews.

XI. SUGGESTED INSTRUCTIONAL STRATEGIES

These are sample instructional strategies, which the teacher can use to accelerate the attainment of the various types of LOs in this course:

a) Massive open online courses (***MOOCs***) may be used to teach various topics/sub topics.
b) About ***30%*** of the ***LUOs*** which are relatively simpler or descriptive in nature that can be understood without the teacher assistance are to be given to the students for ***self- learning(SL)***, but to be progressively assessed for their integration into the ***meso-level*** COs.
c) With respect to ***section No.XII*** teachers need to ensure the attainment of the various ***micro-level outcomes*** by creating opportunities and provisions for ***co-curricular activities***.

XII. SUGGESTED STUDENT ACTIVITIES

Other than the classroom learning, following are some of the suggested student-related ***co-curricular*** activities that can be undertaken to accelerate the attainment of the various LOs of this course:

a) Students form teams to quickly design and demonstrate a digital solution for sequence detectors, parking systems, or password-controlled locks using logic components or HDL within a limited time.
b) Prepare 15 min. power point presentation on digital logic components used in real systems such as calculators, ATMs, washing machines, microcontrollers, or automotive control units.

XIII. COURSE PLAN

This week-by-week course plan for the various sessions through the semester, is mapped with Section VIII and Section IX of this Course Structure and the Micro-project Proposal Template for continuous assessment examination (CIE) in assessing the attainment of the PrOs, LUOs, ADOs and their integration in the micro-project.

Note: Green shaded matter is for self-learning (SL)
The process-related (P) and product-related skills (P) in blue highlights is assessed through every practicum

Unit No. and Unit Title	**Week No.** and Session	**Meso-level LOs and Micro-level LOs**	**Topics and sub-topics**	**T-L Method and Assessment**
Unit – I **Number systems and Minimization Techniques**	**1** (Session 1) *Date….*	Teacher to explain the ***meaning*** of the different ***types of LOs*** in the ***Course Structure*** and how ***students*** should attain to ***exhibit*** the ***LOs*** in the ***CIE*** and ***SEE***		***Course In-charge***
		CO-1: Evaluate the use of number systems and minimization techniques of digital circuit designs.		
	1 (Session 2) *Date…*	**LUO-1a.** ***Interpret the given*** expression in terms of Minterms and Maxterms **LUO-1b.** ***Simplify the given*** Boolean expression.	1.1 Number systems 1.2 Minterms and maxterms expressions	Lecture with PPT, ***Quiz***
	1 (Session 3) *Date…*	Same as above	Same as above	Same as above and ***Tutorial***
		Allocate micro-projects to student groups addressing at least 3 COs	***1st week-end***	***Course In-charge***
	2 (Session 4) *Date…*	**LUO-1c.** ***Design*** a digital logic circuit for ***the given*** application.	1.3. Algebraic method	Lecture with PPT, ***Quiz***
	2 (Session 5) *Date…*	Same as above	Same as above	Same as above
	2 (Session 6) *Date…*	Same as above	1.4 Karnaugh maps (including 5 and 6 variables), don't care condition and Quine McCluskey Minimization Technique.	Same as above and ***Tutorial***
		1st review of micro-project based on action plan activities.	***2nd week-end***	***Rubrics of Micro-Project***
	3 (Session 7) *Date….*	Same as above	Same as above	Same as above
	3 (Session 8) *Date…*	**LUO 1d** ***Design*** a logic circuit for ***the given*** code conversion.	1.5 Codes: BCD, Excess- 3, Gray.	Lecture PPT, Numericals ***Quiz***

Unit No. and Unit Title	Week No. and Session	Meso-level LOs and Micro-level LOs	Topics and sub-topics	T-L Method and Assessment
	(PrO Session **1)** *Date…*	***PrO-1. Design** a code converter for **the given** application.*	Same as above	P and P Assessment
Unit–II **Digital Circuit Design using VHDL**		***CO-2: Develop VHDL designs of various digital systems.***		
	3 (Session 9) *Date……*	**LUO 2a. *Design*** a combinational circuit for ***the given*** Boolean expression using ***the specified*** modelling style.	2.1 VHDL design flow, program structure	Lecture with PPT, ***Quiz***
		2nd review of micro-project based on action plan activities	***3rd week-end***	***Rubrics of Micro-Project***
	4 (Session 10) *Date……*	Same as above	Same as above	Same as above
	(*PrO* Session **2)** *Date……*	***PrO-2. Evolve** a VHDL code for **the given** digital logic circuit*	Same as above	P and P Assessment
	(PrO Session **3)**	***PrO- 3. Design** a digital logic circuit for **the given** code conversion using VHDL.*	Same as above	P and P Assessment
	4 (Session 11) *Date……*	**LUO 2b. *Design*** *a* counter with ***the specified*** Flip flop using ***the given*** modelling style.	2.2 VHDL design elements - structural design elements.	Lecture PPT, Numericals ***Quiz***
	4 (Session 12) *Date……*	Same as above	Same as above	Same as above
	5 (Session 13) *Date……*	Same as above	Same as above	Same as above
	5 (Session 14) *Date……*	**LUO 2c. *Design*** a register with ***the specified*** Flip flops using ***the given*** modelling style **LUO 2d. *Design*** the memory blocks for ***the given*** specification.	2.3 Data flow design elements, behavioral design elements 2.4 Memory functions and procedures, libraries and packages	Lecture with PPT, Self-study ***Quiz***
	5 (Session 15) *Date……*	Same as above	Same as above	Same as above
	6 (Session 16) *Date……*	Same as above	Same as above	Same as above
		3rd review of micro-project progress by teacher	***5th week-end***	***Rubrics of Micro-Project***
		Test - I	***CIE – 1 for LUOs***	***Pen and Paper Test***
Unit – III **Combinational circuits**		***CO-3. Evaluate performance of digital combinational circuits***		
	6 (Session 17) *Date…*	**LUO 3a. *Interpret the given*** adder and subtractor digital circuit.	3.1. Arithmetic circuits: adders and subtractor 3.2. Ripple carry adders and Carry look ahead adders	Lecture with PPT, ***Quiz***
	6 (Session 18) *Date……*	Same as above	Same as above	Same as above

Unit No. and Unit Title	Week No. and Session	Meso-level LOs and Micro-level LOs	Topics and sub-topics	T-L Method and Assessment
	7 (Session 19) *Date…*	**LUO 3b.** ***Interpret*** the comparator circuit for ***the given*** application	3.3 Adder cum subtractor, BCD Adder and Subtractor 3.4 Comparator	Lecture with PPT, ***Quiz***
	7 (Session 20) *Date….*	Same as above	Same as above	Same as above
	7 (Session 21) *Date…*	**LUO 3c.** ***Design*** a digital logic circuit using Encoder and Decoder for ***the given*** Boolean expression for ***the specified*** application	3.5 Decoder, Encoder, Priority encoder	Lecture PPT, Numericals ***Quiz***
	8 (Session 22) *Date…*	Same as above	Same as above	Same as above
	(PrO Session **4)** *Date….*	***PrO-4. Design the given*** *adder/ subtractor digital logic circuit using* ***the specified*** *VHDL behavioural architecture code*	Same as above	P and P Assessment
	(PrO Session **5)** *Date….*	***PrO-5. Design the given*** *adder /subtractor digital logic circuit using digital ICs*	Same as above	P and P Assessment
	(PrO Session **6)** *Date….*	***PrO-6. Design*** *digital logic circuit for* ***the given*** *magnitude comparator*	Same as above	P and P Assessment
	8 (Session 23) *Date…*	**LUO 3d.** ***Design*** a Parity generator and checker for ***the specified*** application	3.6 Parity Generator and checker	Lecture with PPTs **Quiz**
	8 (Session 24) *Date…*	Same as above	Same as above	Same as above
	(PrO Session **7)** *Date….*	***PrO-7. Design*** *digital logic circuit for* ***the given*** *generator and checker*	Same as above	P and P Assessment
		4th review of micro-project progress by teacher	***8th week- end***	***Rubrics of Micro-Project***
	9 (Session 25) *Date…*	**LUO 3e.** ***Design*** a digital logic circuit using MUX/ DEMUX for ***the given*** Boolean expression ***the specified*** application **LUO 3f.** ***Design*** a logic circuit using Programmable Logic Design for ***the given*** application.	3.7 MUX/DEMUX and their structures 3.8 logic using ROM array.	Lecture with PPTs Self-study **Quiz**
	9 (Session 26) *Date…*	Same as above	Same as above	Same as above and Tutorial
	(PrO Session **8)** *Date….*	***PrO-8. Test*** *the performance of* ***the given*** *MUX \ DEMUX using VHDL programming.*	Same as above	P and P Assessment
	(PrO Session **9)** *Date…*	***PrO-9. Test*** *the performance of* ***the given*** *MUX/ DEMUX using IC 74153 / IC 74139.*	Same as above	P and P Assessment
Unit–IV **Sequential circuits**		***CO4. Evaluate performance of digital sequential circuits..***		
	9 (Session 27) *Date…*	**LUO 4a.** ***Justify*** the choice of sequential circuit for ***the given*** application.	4.1. Latches and Flip-Flops, triggering methods	Lecture with PPT, ***Quiz***

Unit No. and Unit Title	Week No. and Session	Meso-level LOs and Micro-level LOs	Topics and sub-topics	T-L Method and Assessment
	10 (Session 28) *Date…*	Same as above	Same as above	Same as above
	10 (Session 29) *Date*	**LUO 4b.** ***Modify*** the working of ***the given*** flip-flop for ***the specified*** requirement in ***the given*** scenario.	4.2 Flip-Flop conversion, Excitation Table, state diagram and applications	Same as above
	10 (Session 30) *Date*	Same as above	Same as above	Same as above
	(***PrO*** Session **10**) *Date…*	***PrO-10. Evaluate*** *the performance of* ***the given*** *Flip Flops.*	Same as above	P and P Assessment
	11 (Session 31) *Date……*	**LUO 4c.** ***Modify*** the working of ***the given*** synchronous/ asynchronous circuits for ***the specified*** requirement in ***the given*** scenario. **LUO 4d.** ***Design*** ***the given*** shift registers using ***the specified*** flip flops for ***the required*** application.	4.3. Synchronous and asynchronous circuits 4.4. shift registers,	Lecture PPT, Numericals ***Quiz***
	11 (Session 32) *Date…*	Same as above	Same as above	Same as above and ***Tutorial***
	11 (Session 33) *Date…*	Same as above	Same as above	Same as above and
	12 (Session 34) *Date….*	**LUO 4e.** ***Justify*** the choice of ***the given*** counter for ***the specified*** scenario	4.5 counters	Same as above and
	12 (Session 35) *Date……*	Same as above	Same as above	Same as above
	(***PrO*** Session **11**) *Date…*	***PrO-11. Test*** *the functionality of* ***the given*** *7-segment static display system for dislaying numbers 0 to 9.*	Same as above	P and P Assessment
		Test - II	***CIE – 2 for LUOs***	***Pen and Paper Test***
Unit–V **Finite State Machines**		***CO-5. Evaluate the designs of the Counters and Finite State Machines***		
	12 (Session 36) *Date……*	**LUO 5a.** ***Design*** a synchronous sequential counter digital logic circuit for ***the given*** count value.	5.1 Design of counters using sequential circuit approach	Lecture with PPT, ***Quiz***
		5th review of micro-project progress by teacher	***12th week- end***	***Rubrics of Micro-Project***
	13 (Session 37) *Date……*	Same as above	Same as above	Same as above and ***Tutorial***
	13 (Session 38) *Date……*	**LUO 5b.** ***Design*** an asynchronous sequential counter digital logic circuit for ***the given*** count/MOD value.	5.2 Analysis and synthesis of asynchronous sequential circuits	Lecture with PPT, ***Quiz***
	13 (Session 39) *Date…*	Same as above	Same as above	Same as above and ***Tutorial***
	(***PrO*** Session **12**)	***PrO-12. Design*** an Asynchronous counter for ***the given*** MOD value.	Same as above	P and P Assessment

Unit No. and Unit Title	Week No. and Session	Meso-level LOs and Micro-level LOs	Topics and sub-topics	T-L Method and Assessment
	Date……			
	14 (Session 40) *Date…*	**LUO *5c.* *Design*** a counter for ***the given*** count values using ***the specified*** model.	5.3 Finite State Machines: Mealy Basic design steps, Moore types, Basic design steps	Lecture with PPT, ***Quiz***
	14 (Session 41) *Date…*	Same as above	Same as above	Same as above and Tutorial
	(***PrO*** Session **13**) *Date……*	***PrO-13. Design*** Ring and Jhonson Counter for ***the given*** specification.	Same as above	P and P Assessment
	14 (Session 42) *Date……*	**LUO *5d.* *Design*** a counter for ***the given*** application using state reduction and state assignment. **LUO *5e.* *Interpret*** the hazard that occur in ***the given*** digital circuit.	5.4 State reduction and state assignment 5.5 Hazards.	Lecture with PPT, Self-study ***Quiz***
	15 (Session 43) *Date……*	Same as above	Same as above	Same as above and ***Tutorial***
	15 (Session 44) *Date……*	Same as above	Same as above	Same as above
	15 (Session 45) *Date……*	Same as above	Same as above	Same as above
	(***PrO*** Session **14**) *Date……*	***PrO-14. Design*** an up and down counter for ***the given*** count using VHDL programming	Same as above	P and P Assessment
	(***PrO*** Session **15**) *Date……*	***PrO-15. Design*** a shift register for ***the given*** expression using VHDL programming.	Same as above	P and P Assessment
		CIE: Final Assessment of COs and competency attainment through micro-project	***Seminar*** *and* ***submission*** *of the* ***final micro-project.***	***Rubrics of Micro-Project***

XIV. SUGGESTED BOOKS

S. No.	Title of Book	Author	Publication, Place including ISBN
1	Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog	Morris Mano and Michael D. Ciletti	Pearson Education, New Delhi 2018 **ISBN**-10 9353062012
2	Modern Digital Electronics	R. P. Jain	Mc-Graw Hill Education Pvt. Limited New Delhi, 2019 **ISBN**-10.9355321775
3	Digital fundamentals	Floyd, Thomas L.	Pearson Education, New Delhi, 2019, **ISBN**- 8129707195
4	VHDL primer	Bhasker, J.	Pearson Education, New Delhi, 202, **ISBN**- 9789332557161

XV. SUGGESTED SOFTWARE-BASED LEARNING RESOURCES

The following software-based learning resources is to motivate the students to undertake self-learning using various learning resources (LRs) providing greater insights of various concepts and principles.

S. No.	Description of MOOCs/ NPTEL/ Coursera/ OERs/YouTube and others	Related Link
1	Digital System Design IIT Madras - NPTEL Video	Introduction - Digital System Design - YouTube
2	Digital Design with Verilog IIT Guwahati - NPTEL Video	Digital Design with Verilog: [Introduction Video] - YouTube
3	Digital Circuits by Prof. Santanu Chattopadhyay IIT Kharagpur	Digital Circuits by Prof. Santanu Chattopadhyay - YouTube

XVI. COURSE ARTICULATION MATRIX

Course Code	Semester I Digital Logic Design with VHDL	POs											PSO-1: Integrate the hardware and software co-designs for Embedded systems and IoT applications to achieve optimal performance	PSO-2 Optimize Next Generation Communication Systems	PSO-3: Evaluate the VLSI circuits and systems, to ensure optimal performance
		PO 1 Engineering knowledge	PO 2 Problem analysis	PO3. Design/ Development of Solutions	PO4. Conduct Investigations of Complex Problems	PO5. Engineering Tool Usage	PO6. The Engineer and the World	PO7 Ethics	PO8 Individual and Collaborative Team work	PO9. Communication	PO10. Project Management and Finance	PO11. Life-Long Learning			
	Professional Competency and COs	**Mark** '3'= high, '2'= medium or **'1'**= for the relevant correlation of each PO or PSO, Professional Competency, COs													
E2ECA2540 2	***Professional Competency*** ***Evaluate*** *the performance of digital logic circuits with VHDL in various engineering applications.*	***3***	***3***	***3***	***2***	***3***			***2***			***1***	***1***	3	2
E2ECA2 5402 -1	***CO-1***. ***Evaluate*** the use of number systems and minimization techniques of digital circuit designs	3	3	2	1	1			2			1	1	3	2
E2ECA2 5402 -2	***CO-2***. ***Develop*** VHDL designs of various digital systems	3	2	3	2	3			2			1	1	3	2
E2ECA2 5402-3	***CO-3***. ***Evaluate*** performance of digital combinational circuits	3	3	2	2	2			2			1	1	3	2
E2ECA2 5402-4	***CO-4***. ***Evaluate*** performance of digital sequential circuits	3	3	2	2	2			2			1	1	3	2
E2ECA2 5402 -5	***CO-5***. ***Evaluate*** the design of the counters and Finite State Machines	3	3	3	2	2			2			1	1	3	2

XVII. COURSE STRUCTURE DEVELOPMENT TEAM

1. 'MNO'……Department of ……..
2. 'PQR'…….Department of ……..
3. Head of the Department of ……..

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Annexure - 8

Unique Curricular Features of OBCFC "Alliance Model 2025" v/s Other Current OBE Curriculum Models

S. No.	Essential OBE Curricular Features	"OBCFC Alliance Model 2025" (Refer **Annexures 6 and 7)**	Other OBE Curricula Models (Refer **Annexures 2 and 3)**
1	Is the Curriculum Student-Friendly?	**Yes, e**vident in Annexure-6 and Annexure-7	Hardly
2	Is the Curriculum Industry-Aligned?	**Yes,** evident in Annexure-6 and Annexure-7	No
3	Certification Level as required by NEP-2020.	**Yes,** see 1st row of table in Annexure-6	No
4	Presence of Multi-entry Multi-exit (ME-ME) option as required by NEP-2020 promulgation.	**Yes,** see last sentence of Annexure-6	Not evident

S. No.	Essential OBE Curricular Features	"OBCFC Alliance Model 2025" (Refer **Annexures 6 and 7)**	Other OBE Curricula Models (Refer **Annexures 2 and 3)**
5	Presence of industry-specific *Global-level* LOs (Learning Outcomes) i.e. PSOs (Programme Specific Outcomes) both in the Programme Structure and Course Structure.	**Yes,** stated in *observable* and *measurable* terms in 1st page of Annexure-6 and Annexure-7	Ambiguous
6	*Assessment strategy* of PSOs in the Programme Structure.	**Yes,** through *Capstone Projects*	Ambiguous
7	Presence of industry-specific *Macro-level* LOs i.e. *Professional Competency* in Programme Structure in the Course Structure.	***Yes,*** stated in *observable* and *measurable* terms in 4th column of Annexure-6 and in ***section II*** of Annexure-7	Absent
8	*Assessment strategy* of Professional Competency related to Cognitive Domain in the Course Structure.	***Yes*** with *Micro-Projects see in* ***section II, III*** and ***X*** of Annexure-7	Absent
9	Presence of industry-specific *Meso-level* LOs i.e. Course Outcomes (COs) in the Course Structure.	***Yes,*** stated in *observable* and *measurable* terms in ***section III*** of Annexure-7	Ambiguously stated
10	*Assessment strategy* of COs in the Course Structure.	***Yes,*** with *Micro-Projects see in* ***section III*** and ***X*** of Annexure-7	Not available
11	Industry-connect of *micro-level* LOs related to Psychomotor Domain i.e. Practical Outcomes (PrOs) of Practicums in the Course Structure.	***Yes,*** stated in *observable* and *measurable* terms in ***section V*** of Annexure-7	No industry connect
12	*Assessment strategy* of *micro-level* LOs related to PrOs or Practicum in the Course Structure.	***Yes,*** stated in in 4th column in ***section V*** of Annexure-7	Not available
13	Industry-connect of *micro-level* LOs related to Affective Domain i.e. Affective Domain Outcomes (ADOs) in the Course Structure.	***Yes,*** stated in *observable* and *measurable* terms in ***section VII*** of Annexure-7	Not stated
14	*Assessment strategy* of *micro-level* LOs related to ADOs or Practicum in the Course Structure.	***Yes,*** see in ***section VII*** of Annexure-7	Not available
15	Industry-connect of *micro-level* LOs related to Cognitive Domain i.e. Learning Unit Outcomes (LUOs) in the Course Structure.	***Yes,*** stated in *observable* and *measurable* terms in ***section VIII*** of Annexure-7	Not stated
16	*Assessment strategy* of *micro-level* LOs related to Cognitive Domain in the Course Structure.	***Yes,*** in TOS of ***section IX*** of Annexure-7	Not available
17	Strategies for inculcating *self-learning* in students in Course Structure.	***Yes,*** highlighted in green in ***section VIII, X*** and ***IX*** of Annexure-7	Not available
18	Course Plan built-into in the Course Structure.	***Yes,*** see ***section XIII*** of Annexure-7	Not available
19	Use of print-based Learning Resources in the Course Structure.	***Yes,*** see ***section XIV*** of Annexure-7	Available
20	Use of software-Based Learning Resources in the Course Structure.	***Yes,*** see ***section XV*** of Annexure-7	Not available
21	Course Articulation Matrix in every Course Structure.	***Yes,*** see ***section XVI*** of Annexure-7	Not available

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