Toward a Fair and Unbiased Debugging Evaluation Instrument

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Introduction

Debugging skills are critical to the semiconductor industry, as deficiencies can incur significant costs. The unpredictable nature of debugging tasks has earned it the nickname “The Schedule Killer” [1] with some electronics engineers spending up to 44% of their time on debugging [2]. Despite the critical economic importance of this million-dollar question [3], undergraduate ECE curricula often omit hardware debugging skills [4], [5]. Instead, it is left to develop indirectly through design projects and labs. To help fill this gap, we are developing a circuit debugging curriculum for undergraduate ECE students. A key component of this effort is creating assessments to qualitatively and quantitatively measure improvements in debugging skills throughout the semester.

In Spring 2024, we conducted a trial of three debugging assessments with 29 undergraduate students to establish baseline debugging skills before introducing the new curriculum [6]. Although the assessments provided valuable insights, reflective journaling, coding of findings, and student feedback revealed opportunities to reduce bias and minimize stressors in the exam process. The updated exam format was used with 50 students during the Fall 2024 semester and reflected the success of the exam modifications. The assessment was improved by adding ample open space to express thoughts throughout the debugging process, clearly communicating more accommodating time limits, eliminating unintended time sinks, and dedicating space on the handout for recording key measurements. The new student feedback is expected to help with iterative improvements to the assessment format as we prepare for the next research phase.

Background on Assessment Design

Construct-irrelevant variance harms the validity of assessments by introducing variables that do not contribute to measuring the desired outcomes but influence results [7], [8]. A literature review on assessment design identified potential sources of construct-irrelevant variance in the exam formatting to be removed from our debugging exams.

Research on typography in exam materials demonstrates that small changes in font size, margins, and other text features can meaningfully affect legibility; poorly formatted materials in timed exams may lead to validity concerns [9]. A 2009 study in a California middle school found that while typographic adjustments did not improve students’ exam performance, increased whitespace made the exam less intimidating and easier to complete [10]. A 2021 study of 15- and 16-year-old students in England taking a science exam demonstrated that additional whitespace improved performance [11]. Students felt calmer, reduced cognitive load by resting their gaze on blank areas while processing questions, and used the space for scratchwork [11]. When a readable font and text size are used, typography is unlikely to pose further issues; however, including suitable amounts of whitespace is important for accurate student performance results.

Lab-based assessments are a major stressor for undergraduate STEM students, particularly when introducing new assessment styles in a lab setting [12]. Stress and anxiety during exams can

negatively impact performance and introduce construct-irrelevant variance [8]. Reducing unnecessary stressors can help students feel at ease and perform better. Although the research team makes the final decision on changes to the assessment, giving students a voice for change in the assessment design process helps make meaningful improvements and empowers students as active collaborators in their educational journey [13]. The iterative improvements made possible by student feedback each semester reflect an action research approach of our practitioner research done in the classroom [14].

Initial Debugging Exam (Spring 2024)

Exam Format

Three circuits were used in the Spring 2024 debugging exam. Fig. 1 shows a non-inverting amplifier circuit and two buggy implementations. Rotating the TL074 op-amp IC swaps the V_{CC+} and V_{CC-} connections, forcing the output to ground [15]. Using an oscilloscope probe in 10x mode with the oscilloscope set to 1x mode displays a 10x attenuated gain. Fig. 2 shows the Greinacher voltage doubler, and a bug created using diodes with a large voltage drop [16]. For additional details on the buggy circuits used in this exam refer to [17].

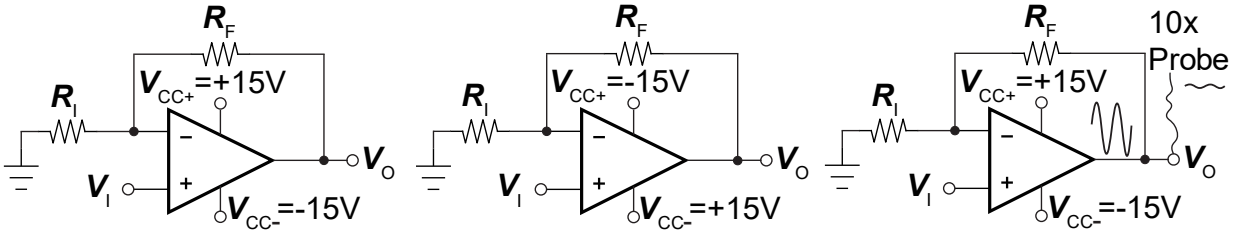

Fig. 1: The functional non-inverting amplifier (left) and the resulting bugs from flipping the amplifier (center) and using the wrong oscilloscope probe settings (right)

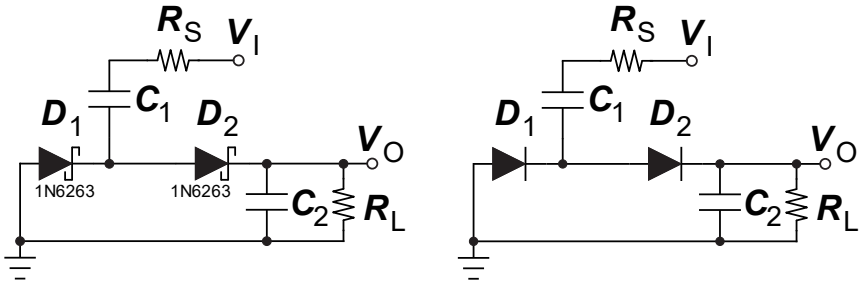

Fig 2: The Greinacher voltage doubler (left) high voltage drop diodes cause a bug (right)

The exam handout for the Spring 2024 semester was printed double-sided on standard 8.5” x 11” paper. Fig. 3 illustrates the general layout of the three debugging problems. The top third of the front page detailed the expected circuit behavior and key input/output values. The rest of the page had space for students to describe discrepancies between measured and expected values, hypothesize root causes, propose fixes, and record the total time spent on the problem. The second page was reserved for student feedback. All text was single-spaced with Times New Roman 12 pt font with no extra space between paragraphs.

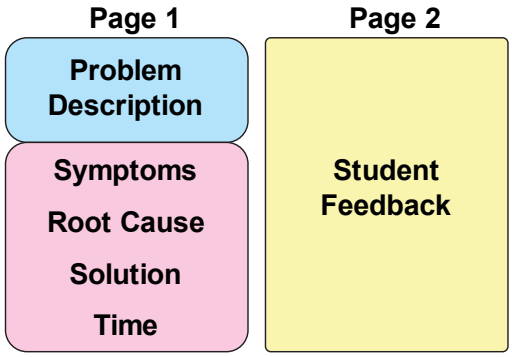

Fig. 3: Layout of the Spring 2024 debugging exam handouts

Student Performance and Challenges

Table I summarizes the students' success rates for the semester, along with conclusions drawn by the research team. The flipped IC problem had a success rate of 31% with eight of 26 students successfully identifying, fixing, and documenting the bug. Another six students (23%) fixed the bug but failed to record their findings. Had these six students documented their findings, the success rate would have been 54%. The confusion students experienced led the research team to revise the exam format for the next semester.

The 10x probe problem was tested with two students. One identified the bug almost immediately, while the other only saw the issue after the exam when they helped clean the lab station. Based on these two results, the problem was deemed suitable for identifying whether students include equipment checks in their debugging problem space.

The incorrect diode bug was deemed unreasonable in its current form. Illegible part numbers made it difficult to identify the incorrect diodes without characterizing the device and cross-referencing datasheets for all diodes in the lab. While this would be a good problem to demonstrate technical knowledge and datasheet literacy, the exam time constraints make this level of analysis and documentation too challenging. The circuit may be reconsidered for future use with visually identifiable diodes to ensure it can be solved within the allotted time.

Table I: Student Success Rates for Spring 2024

Circuit Bug	Success Rate	Comments
Flipped IC	8/26 (31%)	Six students connected the circuit correctly without noting this on the debugging exam. The exam format needs modification so that students do not overlook when they solve the problem.
10x Probe	1/2 (50%)	One student did not complete the problem, the other completed it within 5 minutes. The problem is worth attempting again.
Incorrect Diode	0/1 (0%)	Diode part numbers were found to be unreadable without magnification. The problem requires a redesign before use.

Student feedback and analysis of response patterns informed improvements to the exam format. Twelve students (41%) wrote in the margins or erased work to make space for new findings on the page. Answers were cluttered and key information about the students' thought processes was scattered across the page. Others were brief and lacked key details about their process. To

address these issues, the research team added ***ample space for expression***. Students need space to articulate debugging methodologies such as hand calculations, schematic sketches, and written descriptions of unexpected behaviors. The cramped format may have discouraged students from freely documenting their thought processes, leading them to erase ideas perceived as "irrelevant" or "flawed" and omit key information that would better reflect their understanding of the circuit.

Seven students (24%) said the exam time was too short. Two of these requests came from the first test group, where few students made significant progress within the 15-minute time limit. The research team agreed that the initial time limit was too tight, and another 15 minutes were permitted to continue debugging and documenting their findings. Subsequent test groups were informed at the start of the exam that they could request an additional 15 minutes if needed. Other requests came from students who successfully debugged the circuit but lacked time to thoroughly examine the circuit and those who could not find the bug. The research team concluded that the "15 + 15" minute model provided an ***accommodating time limit***, reducing the construct-irrelevant variance of test anxiety without trivializing the exam. Splitting the time into two segments encouraged students to begin documenting their findings while allowing others to submit their exams without distracting their classmates.

Student feedback identified a way to add meaningful time to the exam without further extending the time limit. Four students (14%) reported spending much of their exam time locating the correct cables for their measurements. Some became frustrated or stressed because their usual cable storage was depleted, and they had to check other stations. The research team determined that ***removing unintended obstacles*** such as collecting cables during the exam could reduce the impact of stress and test anxiety.

Twelve students (41%) did not perform any verification to determine if their proposed solution fixed the circuit. As a final modification to the exam format, the research team added a ***dedicated space for measurements*** and key circuit parameters to encourage students to validate their solutions before submitting the exam.

Refined Debugging Exam (Fall 2024)

Revised Exam Format

Four circuits were used in the Fall 2024 debugging exam. The two non-inverting amplifier circuits from the prior semester were used, along with two new common-source amplifier circuits implemented using the ALD1103 [18]. Fig. 4 shows the common-source amplifier and its two buggy implementations. The first bug involves a floating body connection limiting the circuit's gain, while the second uses a PMOS and the NMOS body connection.

Based on student feedback and the research team's analysis, we developed a new four-page exam handout as shown in Fig. 5. The top half of the first page provides a circuit description and a reminder not to erase any work. The bottom half includes a section to record time spent debugging and a large, empty table for documenting circuit information with spaces for expected values and measured values before and after the fix. The second page is dedicated to recording unusual circuit behaviors. The third page provides sections for identifying the root cause of the

bug and proposing a solution. The fourth page has space for research team comments on the demonstrated fix, a request for students to note any resources they used, student feedback, and a brief demographics questionnaire. All text is formatted in Times New Roman 12 pt font with 1.5 spacing and extra space after each paragraph.

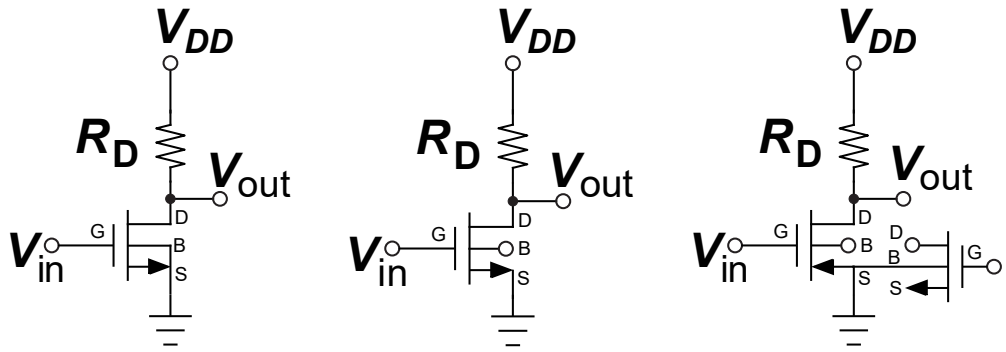

Fig. 4: The common source amplifier (left) and the resulting bugs from disconnecting the body (center) and connecting a PMOS gate, drain, and source with the NMOS body (right)

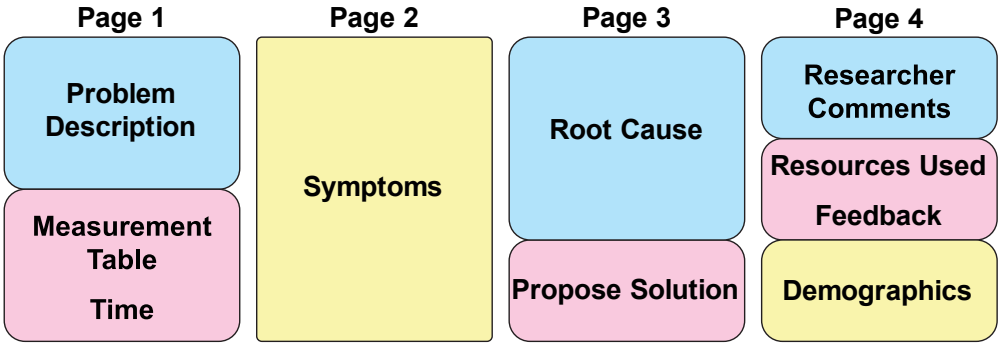

Fig. 5: Updated four-page layout of the Fall 2024 debugging exam handout

Student Performance

Table II summarizes the students' success rates using the new exam format. Notably, the success rate for the flipped IC problem increased to 56%, this is approximately what the prior semester's success rate would have been if all students had documented their power supply connections. For this reason, we attribute the improvement to preset lab stations and additional clarifying text on the exam handout. Differences in students' abilities and understanding of the non-inverting amplifier may have also contributed to the higher success rate.

The 10x probe problem had a success rate of 67%. Three students completed the problem in under 10 minutes by starting with equipment checks. Three others finished between 12 and 27 minutes, including one who discovered the bug accidentally when their finger slipped on the oscilloscope probe. The three students who did not complete the problem never considered equipment in their problem space. This question effectively highlights whether students without prior training recognize test equipment as a potential source of error. However, with debugging skills training, the problem may become trivial, as all students who checked equipment settings first found the problem too easy.

The floating body problem also had a 67% success rate. Many students who fixed the bug found it too easy, noting they had recently completed a lab on the common-source amplifier. Some had encountered floating body connection errors, so they checked IC connections even before testing the output. Others noticed that the schematic required four connections but saw only three on the IC. Students who did not complete the problem often checked the gate, drain, and source connections but incorrectly concluded that a larger resistance or a new IC was needed to achieve the expected gain.

The PMOS circuit had a 100% success rate, with most students describing it as too easy. Multiple incorrect wire placements and the near-unity gain made this bug more apparent during a visual inspection than the other problems. Additionally, the recent common-source amplifier lab further reduced its difficulty. These findings help inform the appropriate difficulty of future exam problems. Given the time constraints of the exam, students need familiarity with the circuit; however, using a circuit covered in class a week or two before the exam may bypass the need to reference IC documentation, oversimplifying the problem.

Table II: Student Success Rates for Fall 2024

Circuit Bug	Success Rate	Comments
Flipped IC	10/18 (56%)	Add instructions to the handout telling students not to adjust the current limit on the power supply.
10x Probe	6/9 (67%)	Debugging training on equipment checks may trivialize this problem as students consider equipment in their problem space.
Floating Body	10/15 (67%)	Students had completed a lab using this circuit only a few weeks before the debugging exam. The recent exposure to the circuit may have made this problem easier to solve.
PMOS	8/8 (100%)	Multiple discrepancies between the schematic and the implementation made this “too easy” to most students.

Impact of Exam Format Changes

The results from the Fall 2024 semester suggest that the revised exam format was effective. First, 28 students (56%) used the measurement table on the first page to summarize their debugging findings. Including fields for values before and after the fix provided insights into which students submitted their answers without critically evaluating their results.

The four-page handout with increased whitespace and ample space for expression also improved student responses. 22 students (44%) wrote substantially more about their debugging process than the original document could accommodate. While others wrote an amount that could fit on the original document, the additional space between different thoughts made it easier for the research team to follow their debugging processes. Only one of the fifty students wrote in the margins and erased work. The extra space may add meaningful debugging time to the exam without extending the time limit by removing potential concerns of running out of space.

Seven students (14%) still indicated that more time was needed. The requests came from students who could not identify the bug and those who found it near the 30-minute mark. The reduced percentage of time-extension requests suggests that time-saving measures improved the

exam's quality. While the "15 + 15" time limit was generally effective, with fewer students exhibiting signs of stress and anxiety, feedback and observations revealed additional avenues that may further reduce construct-irrelevant variance related to exam timing.

Future Work

We collected 50 students' results in the first semester using our improved assessment format. In the upcoming semesters, we will administer the improved format to further validate and strengthen our findings. We remain committed to giving students a voice in the assessment's development by refining the format based on their feedback.

The op-amp problems were implemented on a PCB, while the common-source amplifier problems used a breadboard. Of the 27 students who worked with a PCB, eight (30%) mentioned difficulty reading the PCB in their feedback. Components were on the top of the unlabeled PCB, with traces on the bottom. One student found it difficult to "look underneath for connections and flip it in your head," and others were impeded by the cables and probes attached. To address this, the research team plans to design a PCB with silkscreen labels for the test points to evaluate how clearer labeling impacts students' debugging methodology.

Five students expressed uncertainty about permissible modifications to the circuit and lab setup. Explicitly stating any prohibited changes in the exam instructions may help students begin debugging more confidently and efficiently. For example, the next exam version will clarify that students are not to cycle power on any test equipment, as research team members observed that current limits were being reset from 15 mA to 1 A, potentially damaging ICs.

One student debugging the flipped IC problem noted that the "TL074 datasheet would have been helpful; however, I was able to debug using the pinmap provided in this document." This feedback raises a potential concern that including the pinout may have unintentionally hinted at the importance of pin orientation. An alternative may be to provide all necessary datasheets on the course Canvas page and tell students to bring a device for datasheet access. This change would still ensure access to the required information while expecting better datasheet interpretation skills to debug the circuit successfully.

Conclusion

A fair and unbiased debugging exam is central to the next research stage, where formal debugging training will be introduced, and changes in students' debugging skills will be observed before and after training. By incorporating ample space for expressing thoughts throughout the debugging process, communicating a more accommodating time limit, removing unintended time sinks, and adding a dedicated space for recording key measurements, the exam format is better equipped to assess students' debugging abilities. Using observations from the exam and intentionally including student voices in the improvements will refine our exam to improve its validity throughout the research.

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