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Preparing Fab-skilled Engineers for the U.S. Chip Industry Through Hands-on Integrated Circuit Fabrication

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Abstract: The semiconductor industry is critical to the U.S. economy, driving cutting-edge innovation and technological advancements. In recent years, the United States has faced unprecedented challenges in this sector including supply chain disruptions, shortage of talented and skilled workforce, and intense competition from foreign chip manufacturers. According to the Semiconductor Industry Association (SIA), the U.S. share of global semiconductor manufacturing has dropped significantly, from about 37% in 1990 to approximately 12% in 2023 [1]. In response to this concerning decline, the U.S. government has initiated programs to increase domestic manufacturing, such as the CHIPS and Science Act, which aims to boost advanced chips production in the U.S, prompting an urgent need to bolster workforce readiness [2, 3].

In this paper, we discuss our efforts and experiences in an industry-sponsored project that aims to address this need by preparing 'fab-skilled' engineers through the development and implementation of a lab-based 'Integrated Circuit Fabrication' course. By integrating theoretical knowledge with practical hands-on experience, the course is designed to equip students with the skills necessary to excel in the semiconductor manufacturing industry. This paper outlines the course structure, pedagogical approach, industry and academic partnerships, and expected outcomes. The 'IC Fab' course is implemented at an emerging R2 institution in partnership with a top-tier R1 university. The course includes key topics related to semiconductor manufacturing, and special emphasis is given to the labs and a design project, together accounting for 50% of the course assessment. Students fabricate various discrete semiconductor devices (including p-MOSFET, n-MOSFET, resistors, diodes) and integrated circuits (including, Ring Oscillator, and various CMOS-based logic circuits) on a 2-inch Silicon wafer during 11 laboratory sessions spanned throughout the semester. The labs are conducted in a Class 100 cleanroom and are designed to teach learners the necessary fabrication processes and device characterization steps including photolithography, etching, doping, oxide growth, metallization, and electrical characterization techniques of the fabricated devices and circuits. Through this course, students also become familiar with various microelectronic device manufacturing equipments and facilities, including wet benches, spin rinse dryer, mask aligner, spin coater, diffusion furnaces, physical vapor deposition (PVD) system, reactive ion etching (RIE) system, and various characterization instruments including Hot Probe, Optical Ellipsometer, 4-point Probe Resistivity measurement system, Probe Stations, source-measure units (SMU), and Digital Oscilloscopes.

In this paper, we discuss the anatomy of the course structure, the details of the laboratory exercises, lab infrastructure, and the impact of the course based on our analysis of the student surveys. The survey questions consisted of rating scale and open-response questions to measure knowledge, competency, lab skills, and students' job readiness. Survey results are analyzed quantitatively using statistical indicators such as mean, median, and frequency distribution, and qualitatively using thematic analysis. The course equips students with fundamental concepts of semiconductor fabrication processes, materials science, practical IC design, and device fabrication principles. In addition, students learn industry standards, safety protocols, and basic cleanroom practices. Our

approach in implementing this course can serve as a role model for many other universities to create similar infrastructure to accelerate the training of undergraduates in semiconductor manufacturing, thus creating 'Fab-skilled' engineers to better support the immediate needs of the U.S. semiconductor chip industry.

Introduction:

The semiconductor industry is one of the most vital sectors in the global economy, driving technological innovations that are foundational to our modern society. From enabling the advancements in artificial intelligence, data analytics, and telecommunications, to providing the critical infrastructure for high-performance computing and national security, semiconductors are integral to every aspect of modern life. In 2023, the global semiconductor industry sales was over $525 billion [4]. However, the semiconductor manufacturing industry in the U.S. has been facing numerous challenges that threaten its competitiveness and capacity to meet both domestic and global demand. The U.S. share of global semiconductor manufacturing has been in steady decline for decades, largely due to the shift of production facilities abroad to countries offering lower labor costs, favorable government policies, and greater investment in semiconductor production infrastructure. The rapid decline in the U.S. share of global semiconductor manufacturing—plummeting from approximately 37% in 1990 to just 12% in 2023—has underscored the need for immediate and decisive action [1, 5]. This decline can be attributed to several factors, including increased foreign competition, particularly from countries like Taiwan, South Korea, and China, which have developed significant investments in semiconductor manufacturing infrastructure. Additionally, disruptions caused by the COVID-19 pandemic, chip shortages, and supply chain vulnerabilities have further exacerbated the situation, revealing the critical need for bolstering domestic semiconductor production capabilities.

A major challenge for the U.S. chip manufacturing industry is the shortage of skilled labor [6, 7]. Semiconductor manufacturing is an intricate and highly specialized field requiring deep knowledge of physics, materials science, electronics, nanotechnology, and expertise in complex manufacturing techniques. There is a significant gap between the current workforce's capabilities and the industry's needs, particularly in terms of hands-on fabrication skills. The skills required to operate complex fabrication tools, design semiconductor devices, and maintain cleanroom standards are highly specialized, and the gap between industry needs and available talent is growing. According to the U.S. Department of Commerce, the shortage of qualified semiconductor engineers and technicians has been identified as one of the primary barriers to meeting the nation's semiconductor production goals.

In light of these challenges, the U.S. government has taken steps to bolster domestic semiconductor manufacturing. The CHIPS and Science Act, signed into law in 2022, allocates $52 billion to support semiconductor research, design, and manufacturing within the United States. This historic investment aims to revive semiconductor manufacturing, reduce reliance on foreign supply chains, and create a competitive workforce that can meet the growing demands of the industry. As a result of this thrust, many semiconductor companies are building new chip fabrication factories in the U.S. As a result, skilled workforce development has become extremely important to cater to the

needs of the industry, specifically to support the advanced manufacturing processes required in the semiconductor industry.

This paper presents one such initiative – an Intel-sponsored project that seeks to develop a pipeline of skilled engineers capable of meeting the evolving demands of the U.S. semiconductor industry. In engineering education, hands-on laboratory experiences are extremely beneficial [8-11]. Lab-based learning environments offer students the opportunity to engage directly with materials, equipment, and processes, allowing them to apply theoretical concepts in real-world contexts [12-15]. This paper discusses the development, implementation, and impact of a lab-based 'Integrated Circuit Fabrication' (hereafter, referred to as 'IC Fab') course at Kennesaw State University (an emerging R2 institution). The course is designed to provide students with comprehensive knowledge of semiconductor manufacturing processes, along with hands-on experience in a state-of-the-art cleanroom environment. The course is implemented as part of a collaboration between Kennesaw State University and Georgia Institute of Technology, a top-tier R1 research university in the nation. Through this collaboration, the course aims to prepare the next generation of engineers capable of addressing both the immediate and long-term needs of the U.S. semiconductor industry.

Objectives and Structure of the Paper:

This paper focuses on an innovative educational effort to address the workforce gap in the semiconductor industry. Specifically, it explores the development and implementation of a lab-based 'IC Fab' course for undergraduate students, designed to prepare them with the skills necessary to contribute to the semiconductor manufacturing sector. The course integrates theoretical learning with hands-on laboratory experience, providing students with practical exposure to semiconductor fabrication processes and device characterization in a state-of-the-art cleanroom environment. The following sections of the paper describes the course overview, laboratory exercises and infrastructure, student learning outcomes, and results of our preliminary assessments on the impacts of the course and experiences of the participating students. This initiative, developed at an emerging R2 institution in collaboration with a leading R1 university can serve as a model for future educational programs in the U.S. aimed at preparing fab-skilled engineers. In the following sections, we first provide details of course and topics, the laboratory infrastructure and lab exercises, then discuss the assessment method and our results. Finally, we make concluding remarks with future improvement plans.

Course Overview:

The IC Fab course is a semester-long program developed by an R2 institution in collaboration with an R1 institution. The course combines theoretical instruction with immersive practical experience in semiconductor fabrication. It is designed for undergraduate students enrolled in electrical engineering degree program. The course covers essential topics in semiconductor manufacturing, including semiconductor processing, materials science, device physics, fabrication, and integrated circuit design principles. In this paper, we specifically focus on the course design and learning outcomes of the participating students from Kennesaw State University (KSU). A 2000-level introductory course (core) on Semiconductor Devices was set as the prerequisite for the IC Fab

course. Due to limited seats, students were competitively selected. All participating students had a 'B' or better in the prerequisite semiconductors course. The IC Fab course counted as an elective toward the fulfillment of their degree requirements. Lecture instructions were carried out by faculty at Kennesaw State, whereas the labs were performed at Georgia Tech's cleanroom. Georgia Tech is located within one hour driving distance from KSU. Participating KSU students traveled to Georgia Tech once a week in order to perform the labs for this course. The sponsorship from Intel included stipends for the participating KSU students. The Intel fund also supported the costs of materials and supplies for labs, and compensation of the lab instructors at Georgia Tech.

Table I summarizes the key topics covered in the IC Fab course and the course learning outcomes.

Table I: Course Topics and Learning Outcomes

Topical Outline	Learning Outcomes
Introduction to Semiconductor Materials, Lab safety Crystallography Oxidation Photolithography Diffusion Wet Etching Tech Plasma Processing Metallization Ion Implantation CVD Processes MEMS Processes Device Characterization	• Fabricate CMOS circuitry using a basic CMOS manufacturing procedure. • Perform common fabrication processes used in microelectronics fabrication. • Test integrated circuits and interpret non-ideal behaviors. • Correlate non-ideal IC behavior back to the processes used to fabricate the device under test. • Model IC physical parameters such as junction depth, dopant concentration and modify fabrication process flow designs to improve device performance • Write technical reports related to the laboratory experiences, integrated circuit characterization, and a process design project. • Compile a Process Design Project including analyzing non-ideal performance of fabricated ICs, developing a process flow to improve performance.

Pedagogical Approach: The pedagogical model integrates active learning through hands-on laboratory exercises with traditional lectures. Students engage in a series of structured lab sessions where they fabricate a variety of semiconductor devices, including p-MOSFET, n-MOSFET, resistors, and CMOS logic circuits. Labs form the backbone of the course and account for 50% of the course assessment. The course is designed to promote student engagement, critical thinking, and problem-solving skills by involving them in the entire semiconductor manufacturing process.

Laboratory Exercises and Infrastructure:

The core component of the IC Fab course is an immersive laboratory experience for the learners, which took place in a state-of-the-art Class 100 cleanroom at the R1 university. The cleanroom is equipped with a range of sophisticated tools and instruments required for the fabrication and characterization of semiconductors. The ultimate goal of this project is to build extensive teaching and research capacity in semiconductor manufacturing at the R2 institute in collaboration with the

R1 institution. In this process, the R2 institutions will build the necessary lab infrastructure in steps over the next few years. A new cleanroom facility is currently under construction at the R2 institution which, when opened in 2026, will house the IC Fab labs for the future offerings of this course, thus replicating and fully transitioning the IC Fab labs from the R1 to the R2 institution. The cleanroom facility used for this course (as reported in this paper) is shown in Fig. 1.

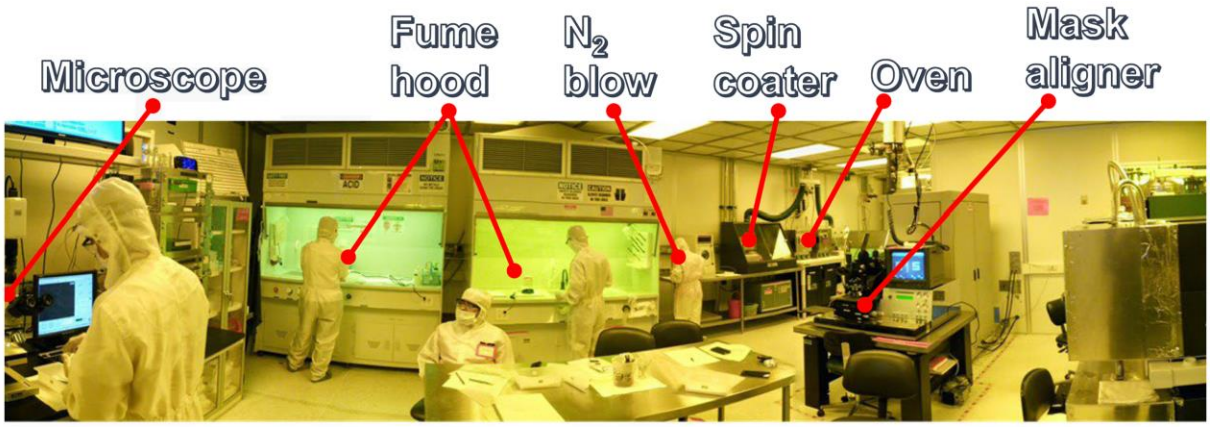

Figure 1. The instructional cleanroom used for this course.

The IC Fab course consists of 11 laboratory sessions, each focused on a different aspect of semiconductor fabrication. Details of the lab sessions and IC fabrication process adopted in this course is provided below.

Lab Session 1: In this lab students perform characterization of the silicon (Si) wafers, perform RCA cleaning of the substrate, perform field oxidation, and measure the field oxide thickness using ellipsometry technique. Before coming to this first lab students are required to review safety information and take a mandatory safety quiz. The resulting wafer at the end of lab 1 is schematically shown in Fig. 2.

Figure 2. Wafer status after Lab 1.

Lab Session 2: In this lab session, the objective is to define the p-well regions on the silicon wafers and selectively open the p-well regions for the following diffusion process. To achieve this, students follow the steps of photolithography, oxide etching, and photoresist removal recipes. The resulting wafer is shown in Fig. 3.

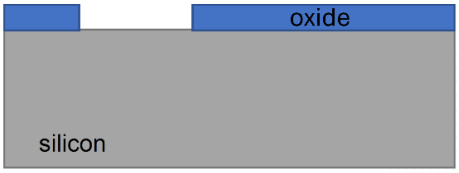

Figure 3. Wafer status after Lab 2.

Lab Session 3: In this lab session, the objective is to diffuse Boron dopants into the p-well regions in silicon wafers using solid dopant sources and then achieve dopant diffusion selectively to p-well regions and measure electrical properties such as sheet resistance. The Boron-doped p-well fabricated at the end of lab 3 is shown in Fig. 4.

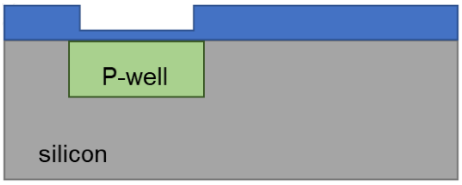

Figure 4. Wafer status after Lab 3.

Lab Session 4: The lab 4 objectives are to define the P^+ source/drain regions on silicon wafers for PMOS fabrication, and then selectively etch the P^+ Source and Drain regions for the following diffusion process. During these processing steps, students use a different mask for the photolithography process and learns the critical mask alignment procedure. The resulting wafer status after completing lab 4 is shown in Fig. 5.

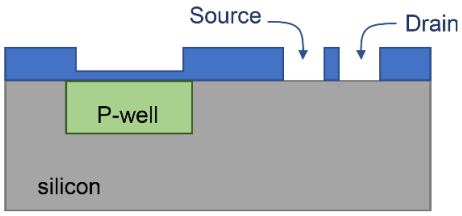

Figure 5. Wafer status after Lab 4.

Lab Session 5: In this lab session, the objectives are to diffuse Boron dopants into the P^+ Source/Drain regions using solid dopant sources and then characterize the electrical properties of the doped regions by using sister test wafers. In this process, students learn how to use a 4-point probe resistivity measurement tool. The resulting wafer status after completing lab 5 is shown in Fig. 6.

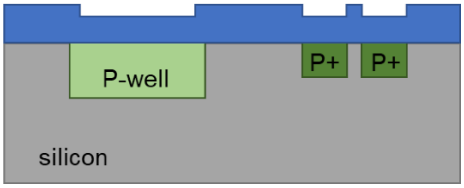

Figure 6. Wafer status after Lab 5.

Lab Session 6: In this lab session, the objectives are to define N^+ source/drain regions on silicon wafers for NMOS fabrication process, and then selectively etch the N^+ S/D regions for the following diffusion process. By the end of lab 6, student have completed total 21 different steps in the fabrication process. Throughout these processes, students use baking ovens, wet benches and make use of chemical resistant personal protective equipments (PPEs).

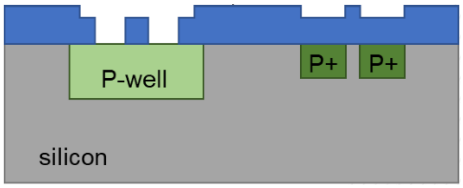

Figure 7. Wafer status after Lab 6.

Lab Session 7: The objectives of lab 7 are to diffuse Phosphorus dopants into N^+ source/drain regions within the p-wells on the silicon wafer using solid dopant sources (Fig. 8), and then to characterize the electrical properties of the doped regions by using test wafers. After this, the wafer is cleaned and prepared for the fabrication of Gate regions of the NMOS and PMOS transistors in the following lab session.

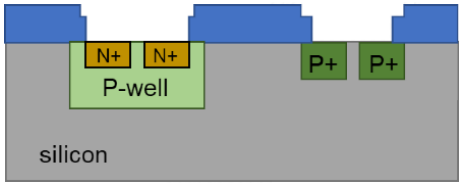

Figure 8. Wafer status after Lab 7.

Lab Session 8: In this lab session, the objective is to grow gate oxide of NMOS and PMOS transistors and to diffuse Phosphorus dopants into N^+ source/drain regions. Following, students characterize the electrical properties of doped regions by using test wafers and make contact/via to the doped regions on the substrate. The resulting wafer after lab 8 is schematically presented in Fig. 9.

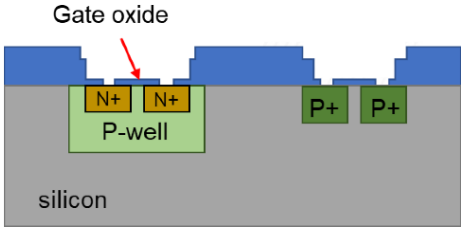

Figure 9. Wafer status after Lab 8.

Lab Session 9: The objectives of this lab session are to make metal contact/via onto doped regions in the substrate and to interconnect devices with metal layer. A physical vapor deposition (PVD) system is used to deposit the aluminum contacts. The resulting wafer is shown in Fig. 10.

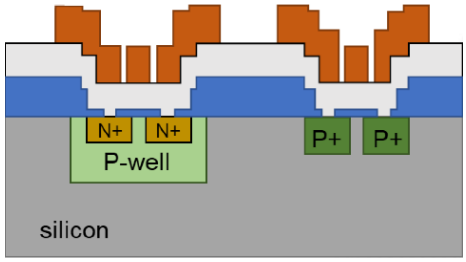

Figure 10. Wafer status after Lab 8.

Lab Session 10: In this lab session, the objectives are to remove remaining photoresists, perform plasma cleaning and anneal to achieve good ohmic contacts. This is the last lab for fabrication, The final device structure and a photograph of the wafer with fabricated CMOS chips/die are shown in Fig 11 below.

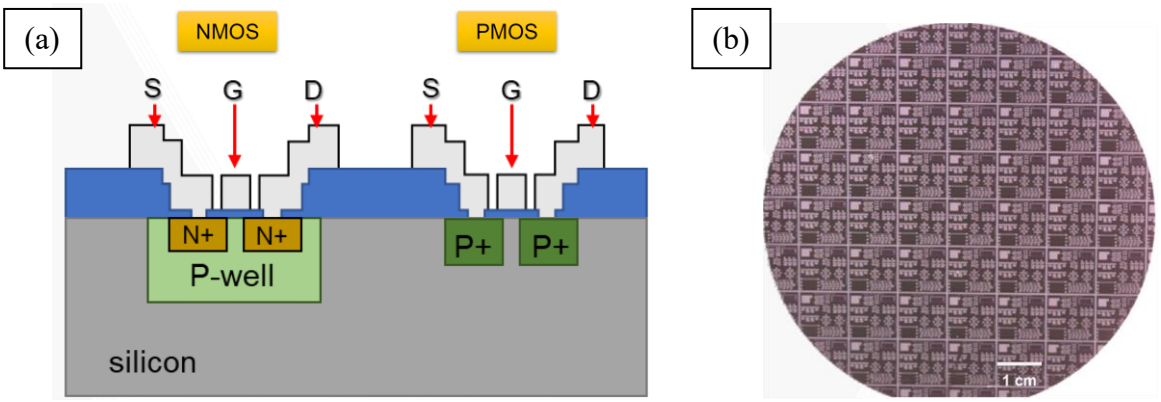

Figure 11. (a) Wafer status after Lab 10, (b) Photograph of a sample wafer containing 36 complete dies (chips).

Lab Session 11: In this lab session, the objectives are to – (i) test devices directly from wafers by using a probe station and testing instruments, (ii) analyze device characteristics and extract DC parameters, and (iii) compare experimental data to analytical/simulation data. In this lab students learn to use probe stations and source measure units to perform current-voltage (I-V) characterization of discrete devices and assess performance of the fabricated CMOS logic circuits. A microscopic picture of the fabricated p-MOSFET and n-MOSFET devices, and p-MOSFET I-V characteristic curves for a 10 µm channel length device are shown in Fig. 12.

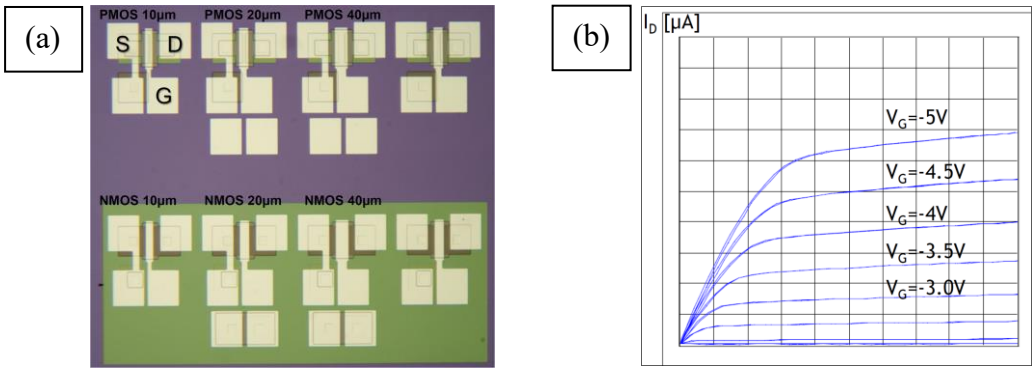

Figure 12. (a) Microscope images of the fabricated p-MOS and n-MOS devices with various channel lengths, (b) sample I-V characteristics of 20 µm p-MOSFETs.

In addition to the discrete MOSFETs, students also characterize Ring Oscillators, CMOS inverters, and NAND logic circuits. A photograph of the fabricated Ring Oscillator (RO) under microscope and its measured electrical characteristics on an oscilloscope are presented in Fig. 13 (a), and 13(b), respectively.

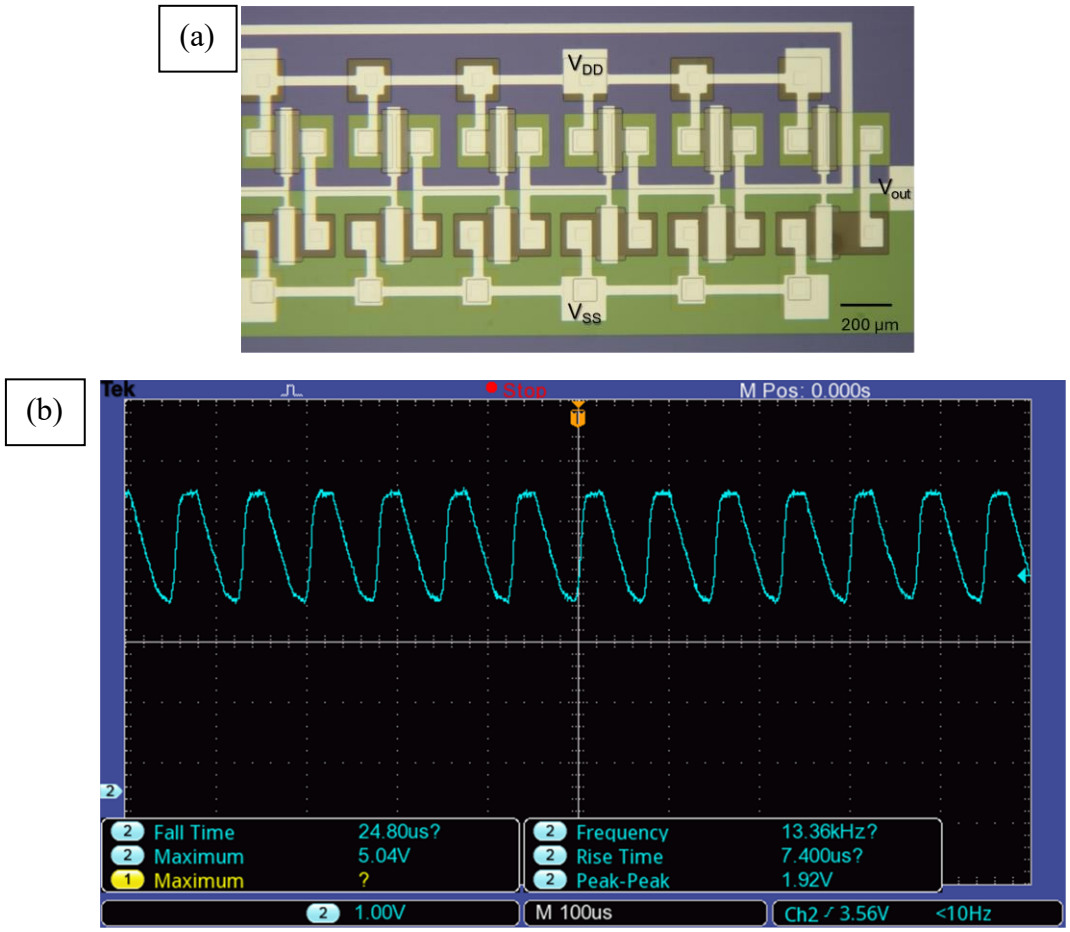

Figure 13. (a) Microscope picture of the Ring Oscillator (RO), (b) Oscilloscope screenshot showing the output characteristics of the RO.

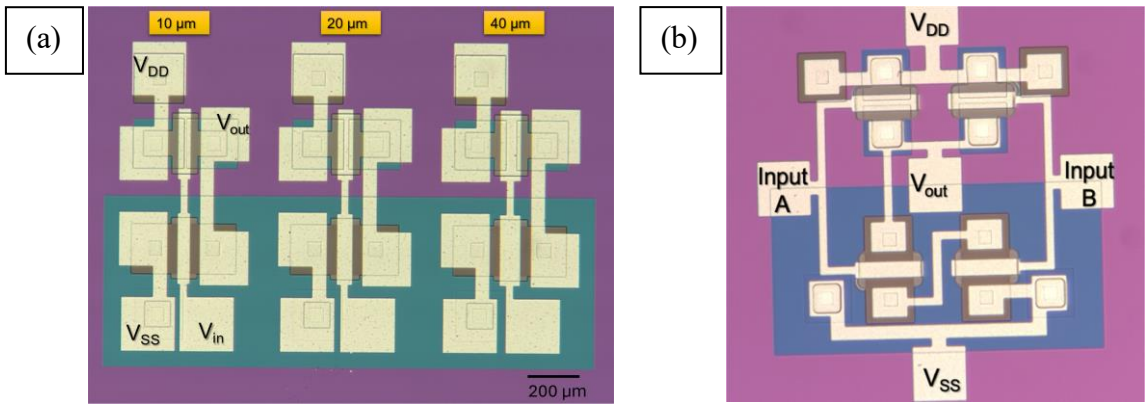

Figure 14. Microscope pictures of the (a) Inverter and (b) NAND logic gates.

Photographs of the fabricated Inverters (NOT gates) and the NAND logic gate circuits are shown in Fig. 14, and their corresponding measured electrical performances are shown in Fig. 14. Inverters with three channel dimensions of 10 µm, 20 µm, and 40 µm were fabricated. As shown in the oscilloscope screenshot of Fig 15 (a), the Inverter circuit flips the 0V (low) and 5V (high) inputs to 5V (high) and 0V (low) outputs, respectively. In Fig. 15(b), the electrical characterization data for the NAND logic gate output is shown for two scenarios – (i) an Input A of "1" (not shown), Input B of "0", resulting in an Output of "1" (high), and (ii) an Input A of "1" (not shown), Input B "1" (high), resulting in an Output of "0" (low).

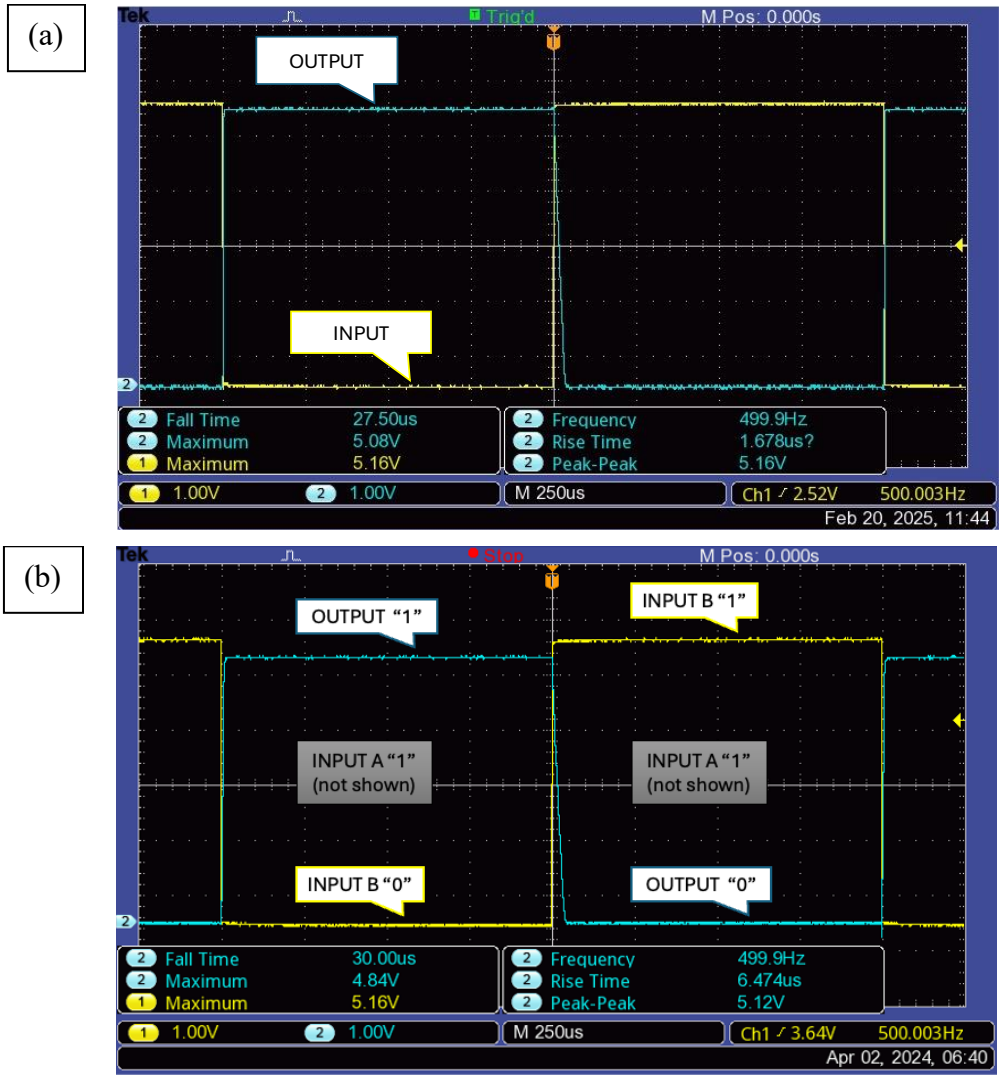

Figure 15. Oscilloscope screenshots of (a) an Inverter and (b) a NAND logic gate.

Assessment Methods:

To evaluate the impact of the course and the hands-on labs, a set of survey questions were designed and administered to the participating students at the end of the fall 2024 semester. Due to the nature of the labs, space limitations, and to maintain safety in the cleanroom, the enrollment was limited to 6. In future semester runs, we are aiming to slightly increase this limit to 8 students per

section/semester. The survey aimed to collect both quantitative and qualitative data to evaluate the impact on student learning, both theoretical knowledge and hands-on microfabrication skills as well as to capture their perceptions on job readiness and growing interest in the semiconductor field. The survey included rating-scale questions and open-ended, free-response questions. This mixed-method approach was chosen to gather objective, measurable data as well as subjective insights into the students' experiences.

Rating Scale Questions: The rating-scale questions were designed to assess students' perceptions of various aspects of the course, including its effectiveness in developing both theoretical and hands-on practical device fabrication skills, influence in raising interest to pursue a future career in the semiconductor industry, and overall satisfaction. These questions required students to quantify their perceptions and input a rating on a 1 to 10-point scale. The responses to these questions were quantitatively analyzed to identify patterns and trends as discussed in the next section.

Free-Response Question: To capture more in-depth insights and identify scopes for future improvements, the survey also included an open-ended question. This question provided students with an opportunity to document their suggestions. The free-response question was aimed to collect qualitative data on the students' experiences and provide insights into potential areas for improvement for future course offerings. The following table lists all the questions in different assessment categories.

Table II: Summary of Survey Questions and Areas of Assessment

Targeted Assessment	Survey Question	Type of Question
Theoretical Knowledge	Before taking the "Integrated Circuit Fabrication" course, what was the level of your theoretical knowledge about integrated circuit/chip fabrication?	Rating-scale
	After taking the IC Fabrication course, to what degree did your theoretical knowledge level increase related to semiconductor device/integrated circuit/chip fabrication?	Rating-scale
Hands-on Fabrication Skills	Before taking this course, what was the level of your hands-on laboratory skills for semiconductor device/integrated circuit fabrication?	Rating-scale
	After taking this course, what is the level of your hands-on laboratory skills for semiconductor device/integrated circuit fabrication?	Rating-scale
Generating Interest in the Semiconductor Field	How much did this course raise your interest in the field of semiconductors and to pursue a career in the semiconductor industry?	Rating-scale
	If offered, to what degree are you interested to take more courses(s) in this area (with hands-on lab-based learning opportunity)?	Rating-scale
	To what degree did this course generate or increase your desire to go to graduate school and enroll into a higher degree program with a focus in the semiconductor-related area?	Rating-scale

Job Preparedness	Before taking this course, how prepared did you feel to apply for an internship or job position in the semiconductor/chip fabrication industry?	Rating-scale
	After taking this course, how prepared do you feel now to apply for an internship or job position in the semiconductor/chip fabrication industry?	Rating-scale
Learning Resources	How helpful were the learning resources provided in this course?	Rating-scale
Overall Satisfaction	How would you rate your overall lab experience?	Rating-scale
Suggestions for Improvement	Do you have any suggestions for further improvements of this course?	Open-ended

Survey Administration:

The survey was distributed to students at the end of the fall 2024 semester, after the final grades have been published. The survey was voluntary, and 100% of students have responded to the survey request. Students were given sufficient time to complete the survey to ensure they can reflect on their experience thoughtfully, without a rush. The data collected from the rating-scale questions have been analyzed using descriptive statistics (mean and standard deviation) to assess the impact of the course. This allowed us to identify general trends in student perceptions and to assess whether the course met its intended goals. The responses to the open-ended question were analyzed using thematic analysis. This approach involves reading through the responses, identifying themes or patterns, and categorizing these themes to better understand student experiences. Thematic analysis provided deeper insights into how the course was perceived by students, including its strengths and areas for improvements. This research study was approved by Kennesaw State's Institutional Review Board (IRB).

Data Analysis and Assessment Results:

The following bar graphs illustrate the generally positive impacts of the course as assessed by the rating-scale questions. For the questions that assessed students' theoretical knowledge level before and after taking the course, we observed that 100% of students have increased their theoretical knowledge in the field (Fig. 16).

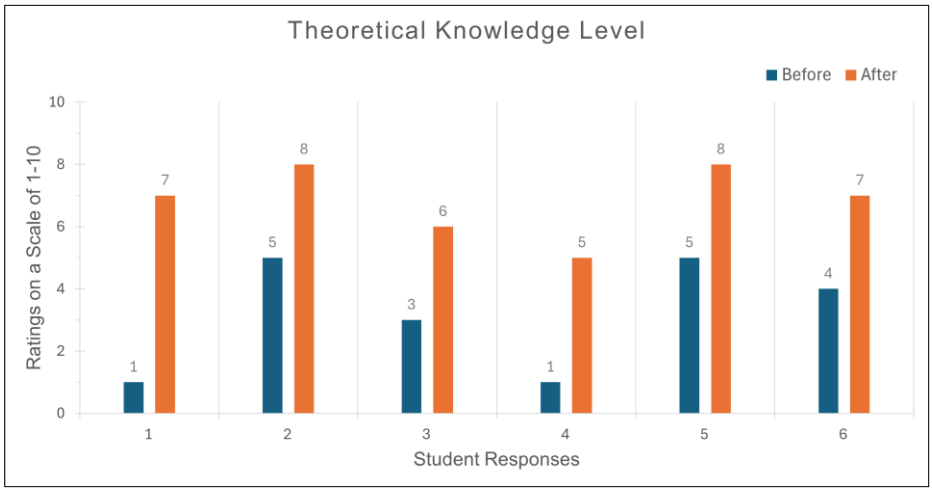

Figure 16. Responses to the Rating-scale questions assessing the impact on theoretical knowledge level.

In this context, we would like to note that the prerequisite for this course was a 2000-level core course on semiconductors, namely Semiconductor Devices. Also, due to seat limitations, the students were enrolled in this course through a competitive application-based process and all enrolled students had earned a grade of B or better in the prerequisite course. It is evident that this newly introduced IC Fabrication course played a significant role in increasing students' theoretical knowledge of semiconductors, even though they have obtained considerable prior knowledge from the prerequisite course. As presented in Fig. 16, the average increase in theoretical knowledge was 3.67 points on the rating scale (equivalent to 232.5% average increase). The two questions assessing the skills in hands-on fabrication before and after resulted in an average increase of 6.67 points (Fig. 17).

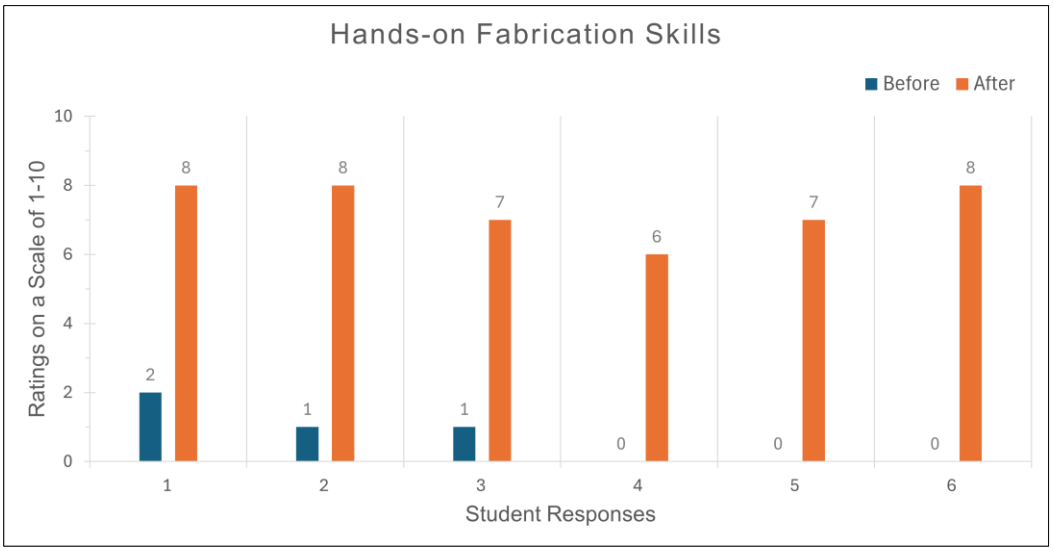

Figure 17. Student responses to Rating-scale questions assessing the impact of the IC Fab course on hands-on device fabrication skills.

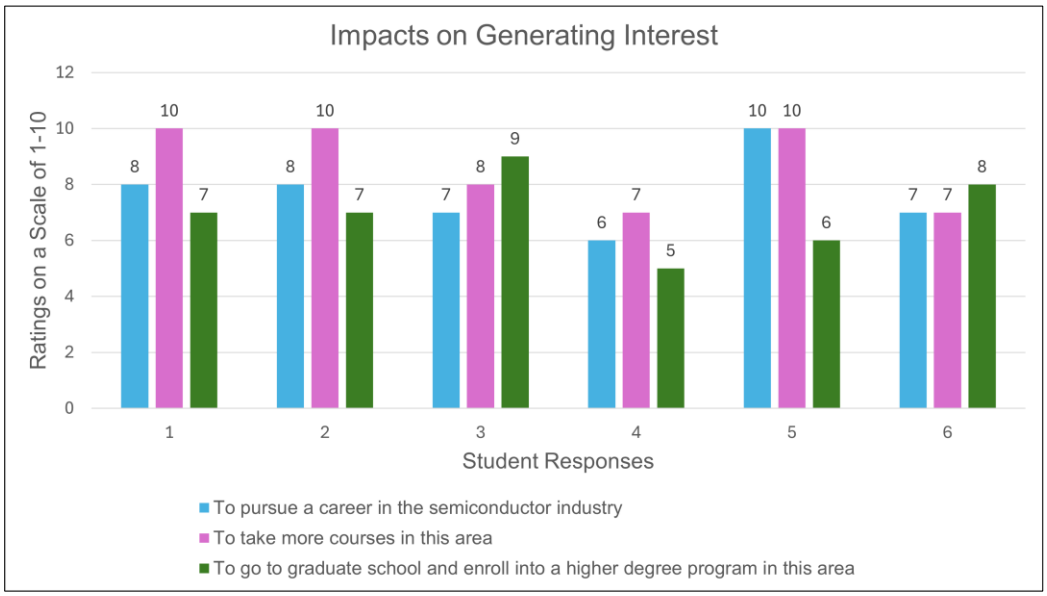

Figure 18. Student responses to Rating-scale questions assessing the impact of the course on raising interest in the semiconductor field.

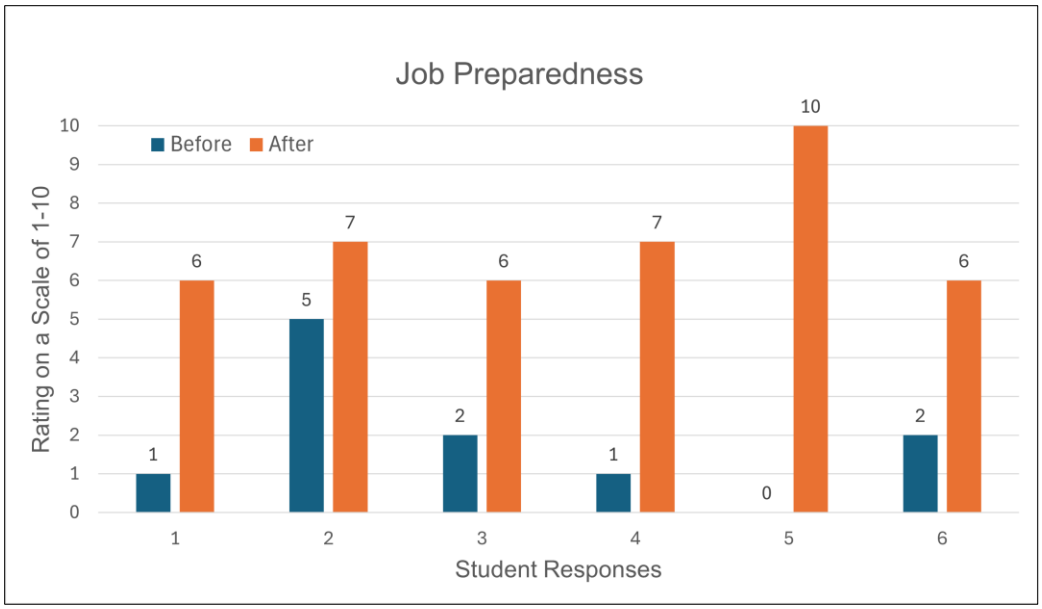

Figure 19. Student responses to the Rating-scale questions assessing perceptions on job preparedness.

The three questions assessing the impact of the course on raising interest in the semiconductor field resulted in average scores of 7.67, 8.67, and 7.0 points, respectively (Fig. 18). Notably, 50% of students have rated 10 out of 10, displaying a high-level of interest in taking more courses in this area. As presented in Fig. 19, the average increase in job preparedness was 5.17 points on the rating scale (equivalent to an average increase of 282.5%).

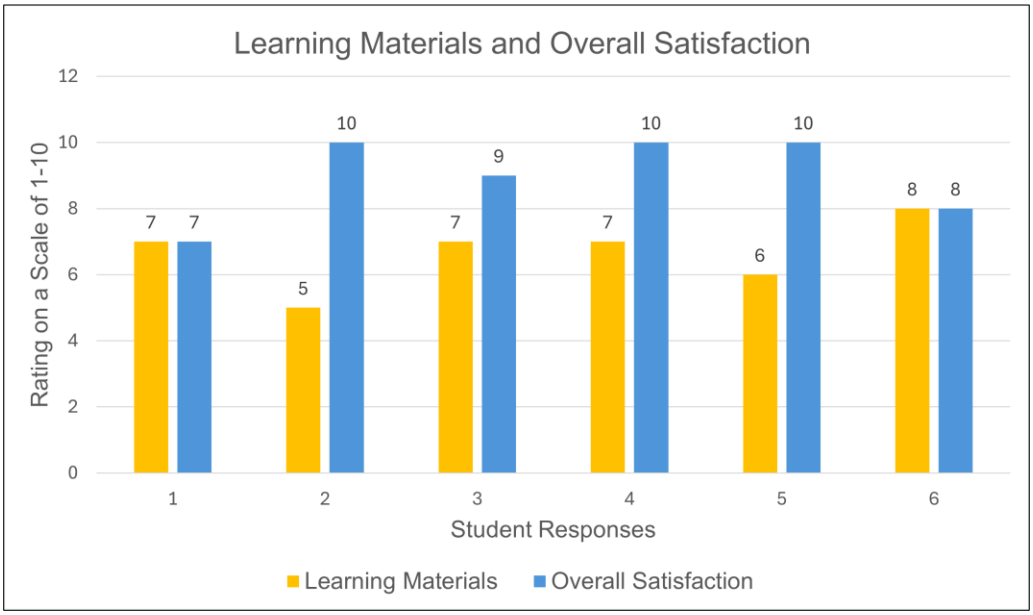

Figure 20. Student responses to Rating-scale questions assessing the effectiveness of the provided learning materials and overall satisfaction with the course.

Participating students have moderately rated the quality of the learning materials provided and indicated a very high level of overall satisfaction with the course (Fig. 20). The mean and standard

deviation of the Rating-Scale responses are summarized in Table III. The mean score considering all questions measuring the course's impact after taking the course was ≈7.5, indicating a strong positive impact. The average values for all questions measuring before and after showed significant increase in the mean value after taking the course. Finally, the mean score for the overall lab experience was 9.0/10 which demonstrates a high degree of satisfaction and positive lab experience by the students. We are currently revising the developed learning materials and working on to create a webpage where the lab manuals, procedures, and sample results will be hosted so that faculty at other institutions can access these for free and leverage on our work for rapid development of similar immersive hands-on experiential courses.

Table III: Statistical Analysis of Rating-Scale Questions

Targeted Assessment	Survey Question	Mean	Standard Deviation
Theoretical Knowledge	Before taking the "Integrated Circuit Fabrication" course, what was the level of your theoretical knowledge about integrated circuit/chip fabrication?	3.17	1.835
	After taking the IC Fabrication course, to what degree did your theoretical knowledge level increase related to semiconductor device/integrated circuit/chip fabrication?	6.83	1.169
Hands-on Fabrication Skills	Before taking this course, what was the level of your hands-on laboratory skills for semiconductor device/integrated circuit fabrication?	0.67	0.816
	After taking this course, what is the level of your hands-on laboratory skills for semiconductor device/integrated circuit fabrication?	7.33	0.816
Generating Interest in the Semiconductor Field	How much did this course raise your interest in the field of semiconductors and to pursue a career in the semiconductor industry?	7.67	1.366
	If offered, to what degree are you interested to take more courses(s) in this area (with hands-on lab-based learning opportunity)?	8.67	1.506
	To what degree did this course generate or increase your desire to go to graduate school and enroll into a higher degree program with a focus in the semiconductor-related area?	7.0	1.414
Job Preparedness	Before taking this course, how prepared did you feel to apply for an internship or job position in the semiconductor/chip fabrication industry?	1.83	1.722
	After taking this course, how prepared do you feel now to apply for an internship or job position in the semiconductor/chip fabrication industry?	7.0	1.549
Learning Resources	How helpful were the learning resources provided in this course?	6.67	1.033
Overall Satisfaction	How would you rate your overall lab experience?	9.0	1.265

The open-ended question asked students to make recommendations for improving the course based on their experience. As shown in the bar chart of Fig. 21, 33.3% of students thought the TCAD software issue could be improved. It is to note that the software currently in use is very old and has compatibility issues with modern operating systems. Other recommendations include providing more example problems (33.33%), improving the learning resources (50.0%)—specifically better lecture slides or more useful textbook. Finally, the fourth recommendation was to make the lectures more interactive in nature to improve the in-class engagement of students.

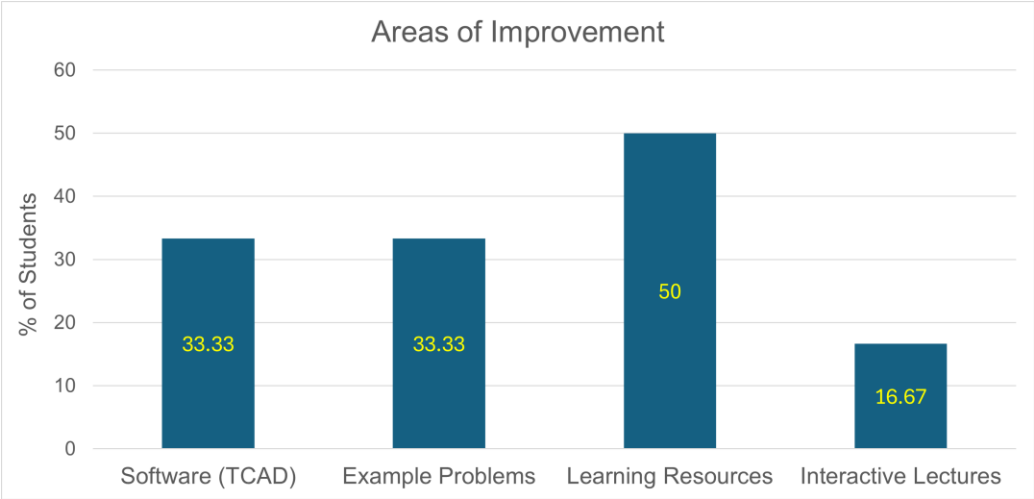

Figure 21. Course improvement recommendations provided by the participating students.

Conclusions:

The course represents a promising development in our curriculum. The course equips students with fundamental concepts of semiconductor fabrication processes, materials science, practical IC design, and device fabrication principles. In addition, students get familiarized with industry standards, safety protocols, and basic cleanroom practices. Our approach in implementing this course can serve as a role model for many other universities to create similar infrastructure to accelerate the training of undergraduates in semiconductor manufacturing, thus creating 'Fab-skilled' engineers to better support the immediate needs of the U.S. semiconductor chip industry.

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