BOARD #132: Further Signal Integrity Experiences in Undergraduate Education

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Further Signal Integrity Experiences in Undergraduate Education [1]

Abstract

Signal integrity has been identified as one of the key areas for scientific education and research at the national level. However, nationally there is a signal and power integrity academic gap. For instance, it has been pointed out by a well-known educator and researcher that: "*The gap between the demand in the industry and the supply of engineers with signal integrity design skills is widening."* Furthermore, having signal/power integrity experiences are of critical importance for Pennsylvania since the Harrisburg metropolitan area has one of the highest concentrations of connector companies in the world.

In addition, our sister campus has received funding to establish a hub under the Creating Helpful Incentives to Produce Semiconductors (CHIPS) Act. As is known, the federal government has budgeted about $280 billion in new funding for domestic research and manufacturing of semiconductors through the CHIPS Act. These new semiconductor chips are tightly packed with signal interconnects densely integrated into small spaces where there exist several coupling mechanisms leading to signal integrity problems. Hence, it is necessary to analyze signal and power integrity, and our campus has expertise in this area. Another important aspect of the CHIPS Act is to develop a skilled a diverse pipeline of workers for building the national semiconductor industry and its associated industries, such as connectors and PCB manufacturing.

In a previous paper, we reported that one of the problems with a signal integrity experience is the type of equipment, such a high-speed sampling oscilloscope and advanced vector network analyzers, that are typically used in the SI laboratory, which tends to be very expensive and beyond the standard laboratory equipment in an undergraduate program. In this paper, we report on the efforts that we have made to keep our signal integrity lab current with new laboratory experiences and capstone projects and undergraduate research. For example, recently, we have obtained support from the Office Naval Research and the local administration to acquire new Vector Network Analyzer to enhance undergraduate/graduate education and research in signal integrity. We have also received a time domain reflectometer (TDR) donation from a local company, and submitted a new Major Research Instrumentation (MRI), National Science Foundation to update the SI Lab. With the updated equipment and software, we also report new student experiences through course projects, funded capstone projects, and internships that keep students current with the advances in the SI.

Furthermore, SI experiences have opened career pathways in a number of local and national companies. We can proudly state that we have graduated over sixty students who have taken a course on signal integrity or have done internships at the signal integrity laboratory and are now working in the SI field worldwide. Furthermore, students highly rated the course (6/7) and provided comments such as "*Lectures and hands-on during labs. The use of many SI equipment and simulation tools plays a big part on understanding the materials*."

[1] The Authors thank the Office of Naval Research (ONR), DURIP Award #: 158263, for their support.

1 Introduction

Technological advancements towards high-speed links have escalated data rates up to 800 Gb/s, in electrical and optical channels[1-5]. This is due to the increasing applications in artificial intelligence, autonomous vehicles, internet of things (IoT), wearables, 5G/6G, machine-to-machine communication, and other data-demanding applications[1-2]. The building blocks for the above applications can be broadly listed as: single-chip and multi-chip integration, integrated photonics and power electronics, MEMS and sensor integration, as well as analog and mixed signals[6-10]. These different blocks must be integrated into PCBs with connectors. Many of these blocks will be working above the 50GHz range, therefore maintaining signal integrity at such high-speed rates is very difficult. Signal integrity means that the signal is unimpaired with regard to its functionality[3]. In a system with interconnects, there are several elements that can impair the signal such as coupling capacitances, ground capacitances, mutual inductances, self-inductances, and wire resistances. These parasitic elements can produce data losses, crosstalk, jitter, and time delays that can significantly degrade system performance and reliability.

In a previous paper[x], we have pointed out that, nationally, there are few universities offering courses in signal integrity at the undergraduate level. For example, at Rose-Hulman Institute of Technology and other institutions, signal integrity modules have been incorporated in existing courses[11-12]. Recently our sister campus started a course on heterogeneous integration and advanced packaging that involves student projects requiring measurement of high-speed channels. Our sister campus is also leading several opportunities related to CHIPS with a focus on signal and power integrity. Our local Penn State Capital College campus has been a leading provider of students with SI skills to the industry. In fact, we have over sixty students who have taken the course and now work in top companies dealing with SI. It is also well-known that high-speed testing equipment is very expensive; hence, we have built the SI lab mainly through external grants.

In addition, in[x] we reported on the development of instructional material and how we delivered efficient laboratory experience with modern equipment (at that time) and software tools for a signal integrity course. In this paper, we report on the efforts made to keep our lab equipment updated, especially with a recently obtained Office of Naval Research (ONR) grant, which will allow us to do research and train students on signal integrity issues up to 67 GHz. This funding was augmented by the local campus administration, depicting their commitment to the overall SI Center activities. We also report on the new experiments developed, internship experiences and capstone projects that we have supervised. Student evaluations of the implemented course are presented and reflect the efficacy of topics and hands-on experiences.

This paper is organized so that in Section 2, we present the course goals and description as well as updated set of experiments. In Section 3, we present samples of student projects, student-based papers and capstone projects to gauge the variety, and the depth of student work. In this section, we also highlight some of the students' comments after taking the signal integrity course. In section 4, conclusions and further work are described.

2. Course Goals and Description and Efforts to Maintain the SI Lab

We started teaching this SI Course as a special topics course (EE 497); it now has a regular denomination within the nomenclature of our university, EE 434[13]. This course provides a solid

foundation in signal integrity for interconnects, the performance of which becomes the key factor in ensuring reliable system operation as the speed of new digital systems is pushed higher into the gigabit range. This course introduces parasitic elements that can impair the signal, such as coupling capacitances, ground capacitances, mutual inductances, self-inductances, and wire resistances. These parasitic elements can produce data losses, crosstalk, jitter, and time delays that can significantly degrade system performance and reliability. Students learn how the characteristics of materials and interconnect layout affect system performance and develop models that can be simulated to verify that performance before production. This course also covers necessary supporting ideas such as transmission line theory, impedance mismatch and reflection, lossy transmission lines, rise time degradation, material properties, crosstalk, and jitter. Students are taught to make and interpret measurements in both the time and frequency domains.

The xxx-metropolitan area, the "Connector Capital of the World," has one the highest concentrations of electrical connector companies in the world. These companies deal with designing and producing interconnects for very high transmission rates. The overall economic impact in the Central xxx Area is estimated at several billion dollars. Furthermore, it has been pointed by a well-known educator and researcher[14] that "*The gap between the demand in the industry and the supply of engineers with signal integrity design skills is widening. This problem is even more critical in the U.S. defense industry where most engineers must be International Traffic in Arms Regulations (ITAR) compliant."* Hence, having signal/power integrity experiences are of critical importance for Penn State Capital College Campus since the Harrisburg metropolitan area has a high concentration of connector companies but also for national defense.

As pointed out, with the significant increase in data rates, connector companies rely on advances in interconnect technology which requires intensive research in signal integrity which not only encompasses electrical engineering but also mechanical engineering, contact physics and material science. Practicing engineers also need a constant update on their skills; hence the authors also have an outreach component by organizing a yearly Central PA Symposium on Signal Integrity that has brought world-leading experts to the area from top industries and academia, such as Northrop Grumman Mission Systems, Intel, IBM, Qualcomm, Molex, Innovium, Rogers Corporation, Samtec, TE Connectivity, Amphenol, Missouri University of Science and Technology, and the University of South Carolina among others.

The authors strongly believe that signal integrity must include meaningful hand-on experiences with equipment most likely found in the industry. Fortunately, the Center for Signal Integrity, at xxx, is equipped for the electrical design and testing of high-speed interconnects. The current lab consists of four VNAs up to 8 GHz, two 20 GHz TDRs, and one BERT 32 Gbps system. Based on the success of the course, the internship opportunities provided by the Center as well as the research stream, the authors in the next section detail the efforts made to maintain and upgrade the SI lab capabilities.

2.1 Efforts to Maintain the SI Lab

The authors have tirelessly worked on grant submission and connection with industry as well as drawing support from the college administration. For example, we have recently received a

$282,770 funding from the Defense University Research Instrumentation Program (DURIP), Office of Naval Research (ONR). This funding, coupled with a $60,000 fund from the college, was used to purchase a new high-end 4-port 67GHz Vector Network Analyzer that will support the ongoing research and teaching activities of the college's Center for Signal Integrity. We have also submitted a proposal to the National Science Foundation, through the Major Research Instrumentation (MRI) program, to upgrade the 32 Gbps bit error rate tester (BERT) that we currently have. Furthermore, we have received a TDR donation from a local connector company. We note that we worked closely with the local connector industry and have full support from the local administration to support the student experiences as well as to keep students current in the SI field.

2.2 Updated Partial List of Laboratory Experiments

Based on our experience, and the updated equipment and software described above, we list the updated set of laboratory experiments from[14], which reflects the influence of the constant advances on the field.

1. Why signal integrity is important
2. Understanding How Ferrites Can Prevent and Eliminate RF
3. Introduction to Keysight ADS circuit simulation tools
4. Using the O-Scope as Time Domain Reflectometer (TDR)
5. ADS Procedure to Obtain S-Parameters of a Passive Device
6. Impedance and Time Delay of a Transmission Line
7. Using a two-port Vector Network Analyzer to Measure S-parameters
8. Using MATLAB Scripts for S-parameter analysis
9. Using the Time Domain Reflectometer (TDR)
10. Designing a Microstrip Line Using High-Frequency Structure Simulator (HFSS)
11. Measuring crosstalk using a TDR, and simulating crosstalk on ADS
12. Using a four port VNA to measure S-parameters
13. Using a Bit Error Rate Tester to analyze a Communication Channel

3. Student Projects and Experiences

To gauge student experiences and the depth and the variety of work done by the students who have taken the SI course, we present a sample of student projects below. These projects include mechanical calibration up to 67 GHz, which is a very important measurement skill. The second project shows students using high frequency simulation software by creating 5 and 9-layer substrate using vias and obtaining insertion and return loss. The last project demonstrates a nondestructive measurement of the dielectric properties of an unknown material by using free space methods.

Four Port Mechanical Calibration

The mechanical calibration kit used for this project was Keysight 85058B 67 GHz 1.85mm STD calibration kit. This kit was used to conduct a Short-Open- Load-Thru (SOLT) calibration. Within the kit, it contains six male standards and six female standards used for calibration: Open, Short 3, Short 4, Short 1, LB Load, and Short 2. These standards are shown in Figure 1 below. It also includes three adapters (male-to-male, female-to- male, and female-to-female) for

thru measurements. The female standards and female-to-female adapters were used on this project.

Figure 1: Mechanical standards within the calibration kit

Figure 2: Calibration set up

To check the calibration, two different thru adapters were used to see if the insertion loss and return loss was acceptable or not. This is shown in Figure 2 below. A signal was sent through each port. The result of the calibration check is shown in Figure 3 below. The insertion loss graph on the top right looks good as it is smooth and very close to zero which is expected as it is just a thru measurement. The return loss in the top left corner looks good as well as it is below or around 30 dB up to 67 GHz which is an acceptable value. Overall, the values for the insertion loss and return loss look good which is a validation of a good calibration.

Figure 3: Measurement Results of device under test with the Calibration

Via S-Parameter Simulations in Keysight ADS

The objective of this project was to use Keysight ADS (Advanced Design System) Via Drawing Utility software for a detailed examination of the worst-case impact of vias on the signal integrity of a signal when traversing a printed circuit board with 5 and 9 layers, respectively. The insights gained from simulation and modeling show the best practices and design strategies for mitigating signal integrity challenges on industry standard PCB layer thicknesses. The first step is to design the 3D model. This is done in the Layout modeler in ADS. In the Layout modeler, the next step is to open the substrate window. In the substrate window, layers are then added until we reach the number of metal layers needed for the simulation. The bottom and top substrate layers are changed to air. All the substrates in between metal layers were set to FR4 with a height of 5 mils. All the metal layers besides the exterior layers were set to slot plane layers. Figures 4 and 5 below show the completed substrate model for the 5-layer and 9-layer 3D models, respectively.

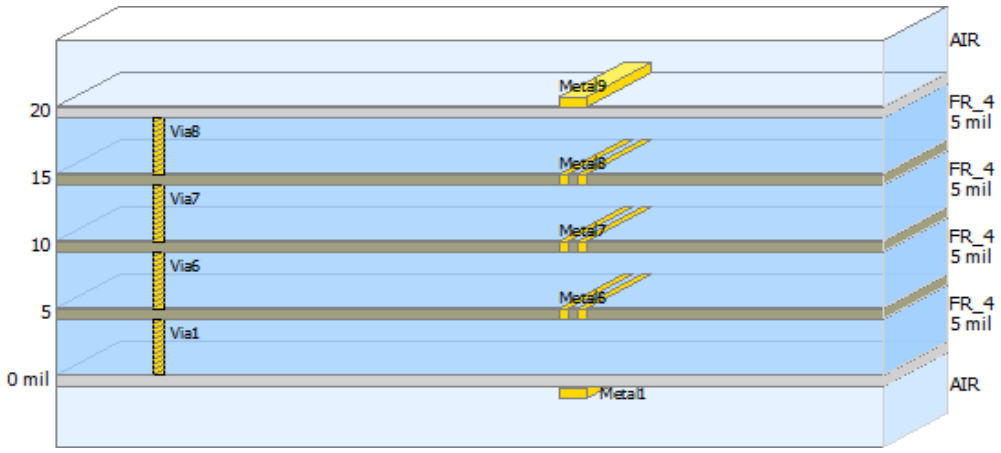

Figure 4. 5-layer PCB substrate model.

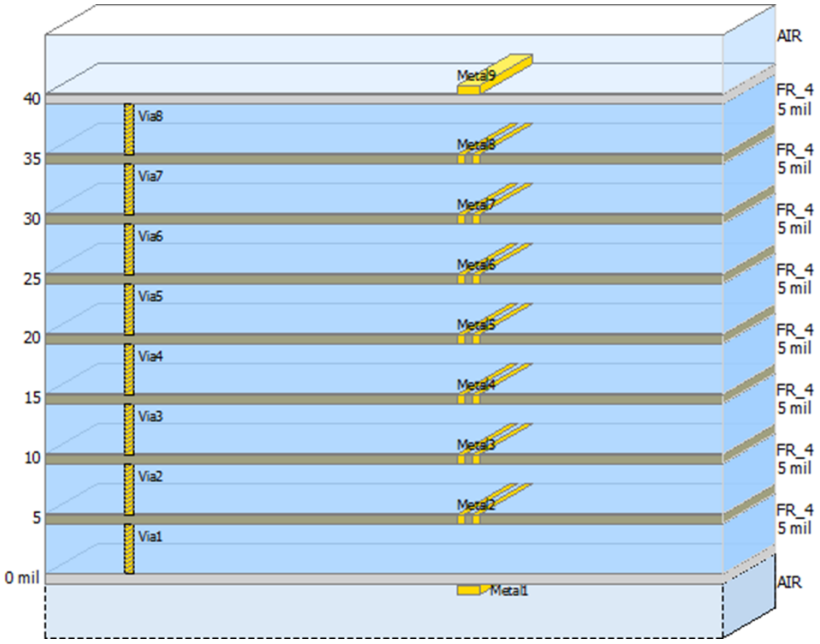

Figure 5. 9-layer PCB substrate model

The insertion loss simulation for the 5 and 9-layer are shown in Figure 6a and 6b respectively.

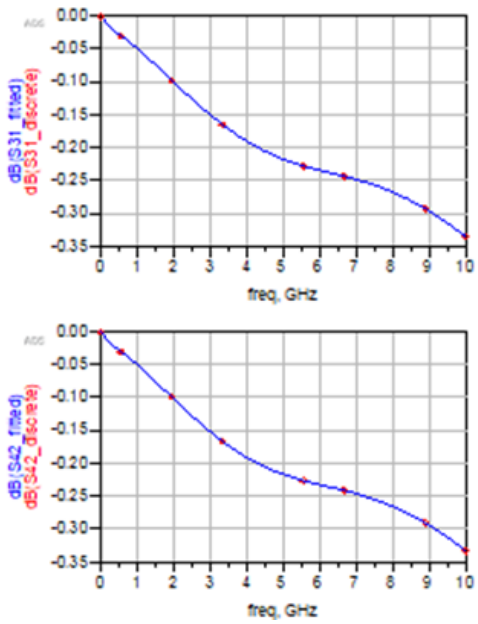

Figure 6a Insertion loss 5-layer

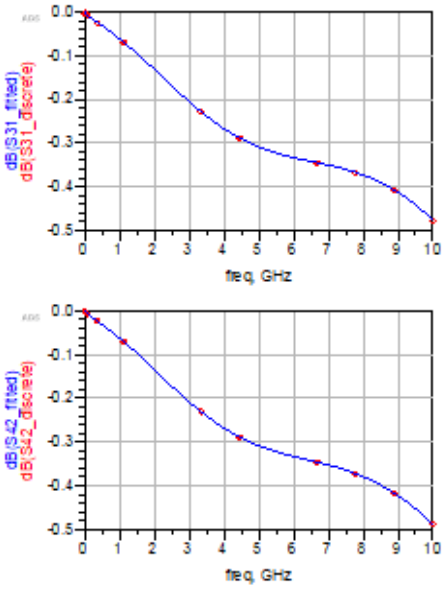

Figure 6b Insertion loss 9-layer

The design phase involved creating a 3D model in the Layout modeler within ADS, encompassing the configuration of substrate layers, metal layers, and the incorporation of vias using the Via Drawing Utility. For both 5-layer and 9-layer PCBs, careful attention was given to the via design, encompassing parameters such as hole diameter, pad diameter, anti-pad diameter, and spacing for the differential signal bias. This process concluded in the construction of the 3D models, with ADS automatically generating and labeling the necessary ports for measuring the vias. The simulation focused on S-parameters, with dB magnitude and phase measurements conducted for both 5-layer and 9-layer PCBs. Notably, the insertion losses for both PCBs remained below 3 dB across the frequency range of 0 to 10 GHz, with the worst insertion losses occurring at 10 GHz. The 9-layer has slightly higher loss due to layer size.

Free Space Measurement of Material Dielectric Characteristics

This experiment involves the nondestructive measurement of the dielectric properties of an unknown material by using free space methods. Through a unique through-reflect-line (TRL) calibration technique and post processing in MATLAB, the material properties were characterized for both a reference piece of Teflon and an unknown material. This measurement technique is an adaptation of the measurement technique illustrated in[15]. Figures 7 and 8 below show the experimental set up utilized.

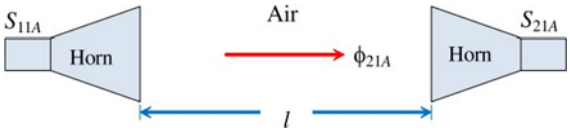

Figure 7: Free Space Measurement Without Sample

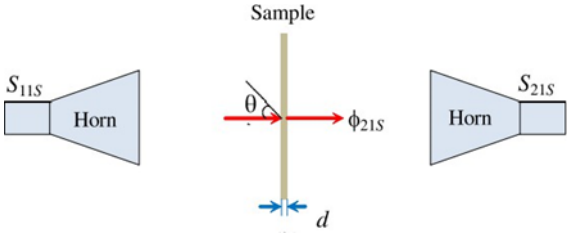

Figure 8: Free Space Measurement with Sample

The following calibration was performed to empirically find the desired distance l. This was performed by placing a metal plate between the two horn antennas, observing the S11 parameter, (see Figure 9), and then the metal plate is moved away from the horn antenna until the S11 magnitude parameter becomes approximately constant, in this case around 0.2. The complete measuring set up with absorbers is shown in Figure 10.

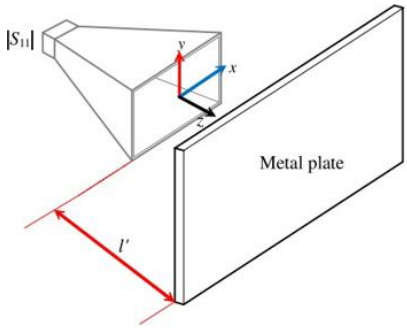

Figure 9: Calibration set up

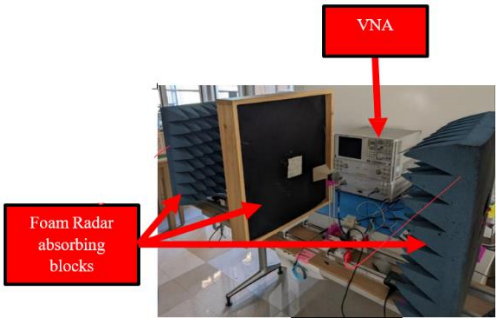

Figure 10: Measuring set up

The set up was used first to measure the dielectric chrematistics of Teflon, which is well-known and of an unknown material. After post processing the measured S-parameters data, the real part of the dielectric constant of Teflon was obtained and is equal to about 2 over the frequency range from 8 to 12 GHz, which matches values on the current literature (see Figures 11a, b), and its loss tangent never went above 0.01, providing confidence on the free space measurement technique. A similar process was followed to obtain the dielectric characteristics of the unknows sample. This sample has a real part of the dielectric constant of approximately 2.7 and a loss tangent of approximately 0.02 (see Figure 12a, b)

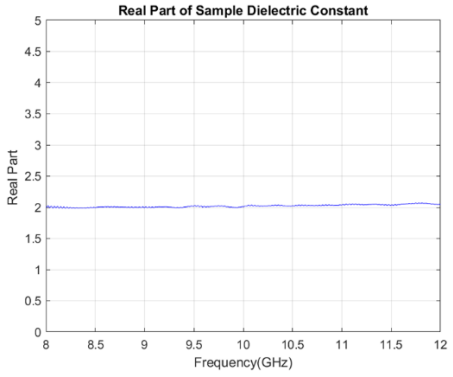

Figure 11 a: Teflon real part of ε_r

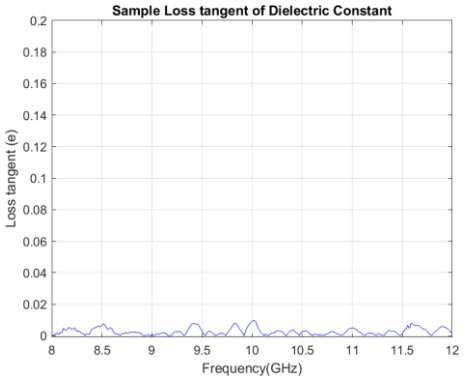

Figure 11 b: Teflon loss tangent

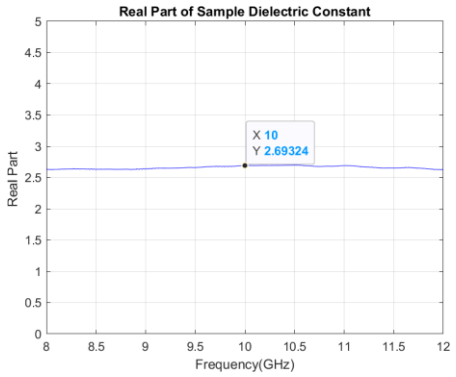

Figure 12a: Unknown sample real part of ε

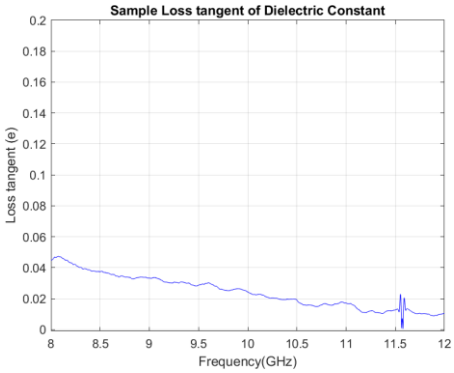

Figure 12b: Unknown sample loss tangent

In addition to the above sample project, there are several other projects such as time domain reflectometer measurements on MIPI D-PHY protocol for signal integrity analysis which resulted in a conference publication[17], as well as internship reports and capstone project supervision. An example of the latter is the Electromagnetic Compatibility and Electromagnetic Interference Evaluation Board. This project was sponsored by Samtec, a connector company. This product allows Samtec to utilize this product as an integral part of measuring the shielding effectiveness of their connectors, as well as distributing valuable information at the customer's request.

Students highly rated the SI course (6/7) and provided comments such as "*Lectures and hands on during labs. The use of many SI equipment and simulation tools plays a big part on understanding the materials*." Or "*The labs were particularly powerful in demonstrating the effects of certain characteristics of a transmission line or other. It created many opportunities to see new equipment and software that is used in modern signal integrity applications and companies."* All of these efforts have led to successful career paths for our alumni. We have graduated over sixty students who have taken a course on signal integrity or have done internships at the signal integrity laboratory and are now working in the SI field worldwide. A partial list of our alumni is available on the Center for Signal Integrity website.

4 Conclusions

In a previous paper, we reported on the development of instructional material and how we delivered efficient laboratory experience with modern equipment and software tools for a signal integrity course. In this paper, we report on the updates that authors have implemented on SI course to keep it current. We also discussed the efforts made to keep our lab equipment updated, especially with a recently obtained Office of Naval Research (ONR) grant, which will allow us to do research and train students on signal integrity issues up to 67 GHz. We note that we have submitted a proposal to the National Science Foundation (through the MRI stream funds) to acquire a new BERT to update the current one to 64 Gbps. We also presented a sample on the new projects that our students developed demonstrating the skills that they learned. Student evaluations of the implemented course were at 6/7, more importantly the comments that they put on the course evaluations were very encouraging. We also noted that practicing engineers can attend our yearly Central PA Symposium on Signal Integrity which has brought world-leading experts to the area from top industries and academia, such as Northrop Grumman Mission Systems, Intel, IBM, Qualcomm, Molex, Innovium, Rogers Corporation, Samtec, TE

Connectivity, Amphenol, Missouri University of Science and Technology, and the University of South Carolina among others, to update their SI skills.

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