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WIP: Strengthening the Semiconductor Workforce Pipeline through Curriculum Development

Dr. Suxia Cui, Prairie View A&M University

Dr. Suxia Cui is a professor in the Department of Electrical and Computer Engineering at Prairie View A&M University (PVAMU). Her research focuses on machine learning, computer vision, cybersecurity, and computing education. Dr. Cui's work is supported by various agencies, including the National Science Foundation, U.S. Department of Agriculture, Department of Defense, and Department of Education. She also leads semiconductor workforce development initiatives at PVAMU through external grants, actively promoting computer hardware and VLSI research and education. Dr. Cui is a senior member of IEEE and a member of HKN, ACM, ASEE, and SPIE.

LUJUN ZHAI, Prairie View A&M University
Dr. Shuza Binzaid

Dr. Shuza Binzaid (PI) is a Research Associate Professor in the SMART center. He has 20 years of experience in various projects for leading and supervising innovative teams of engineers at professional, academic graduate, and undergraduate levels. He has more than 14 years of experience in various fields of energy effects, energy conservation, renewable energy, VLSI microcontroller systems, and automation engineering projects. He is very experienced in the systems-level design of sensors and sensing modules, computational modeling, programming microcontrollers, energy conversion process, and interface design for advanced electronic applications. Also, he has more than 12 technology innovations and 68 technical publications.

WIP: Strengthening the Semiconductor Workforce Pipeline through VLSI Curriculum Enhancement

Abstract

This article highlights an ongoing funded project that provides the Electrical and Computer Engineering department at a minority-serving institution with the resources to: (i) purchase equipment and software licenses to establish a Very Large-Scale Integration (VLSI) Design Laboratory, (ii) train faculty and staff in cutting-edge VLSI techniques, (iii) support graduate students in actively participating in VLSI teaching and research, and (iv) enable tapeout projects in undergraduate and graduate courses.

The project focuses on developing new courses and enhancing existing ones to equip students with the knowledge and skills required for VLSI design and manufacturing. Both undergraduate and graduate courses are involved. At the undergraduate level, "Digital Logic Circuit Laboratory," "Introduction to Digital Design," and "Computer Organization and Design" are core courses for the Computer Engineering degree. Previously, these courses lacked VLSI design content. By integrating VLSI concepts through lectures, labs, and class projects, students can now connect digital theory to chip tapeout across three consecutive semesters. In addition to the undergraduate curriculum enhancements, the graduate-level course "VLSI and ULSI Design" has been revamped to include chip tapeout projects, and a new course, "VLSI Testing and Characterization," has been introduced. This comprehensive training prepares them for careers in the semiconductor industry. Class surveys are used to assess the project's effectiveness.

After two years of implementation, the project team is confident that this initiative will: (i) strengthen the Computer Engineering program at this minority-serving institution, (ii) provide undergraduate and graduate students with valuable hands-on experience in VLSI design, and (iii) support students in securing employment with high-tech companies. In summary, this project will enhance the institution's curricula and contribute to building a more diverse and skilled workforce in the semiconductor industry.

1. Introduction

The new era of advanced computing has not only transformed our daily lives but also introduced new challenges. The demand for faster, smaller, and more efficient electronic devices continues to grow, making semiconductor research and development (R&D) critical to meeting this demand. The CHIPS and Science Act has set a national vision to maintain the United States' leadership in the semiconductor industry [1, 2, 3]. In response, academia and industry are collaborating through innovative efforts to support this vital initiative [4, 5, 6].

Prairie View A&M University (PVAMU) received over million dollars external funding which will satisfy the mission of PVAMU in terms of providing "high-quality educational experience for students who, upon completion of bachelors, masters, or doctorate degrees, possess self-sufficiency and professional competence," particularly in the fields of Digital Design, and Computer Architecture and VLSI Design. The first two years of the initiative focus on developing new courses and enhancing existing ones to equip students with advanced knowledge and skills in VLSI design and manufacturing. Additionally, the program includes practical design tapeout projects to support both VLSI education and research [7, 8].

Beyond curriculum enhancement, the project team has introduced extracurricular activities to further engage students. For instance, a VLSI club was established, serving as a platform for student interaction and collaboration. The team also awarded scholarships to outstanding students, attracting more qualified individuals to pursue careers in this field. Furthermore, a mentoring program is underway, designed to connect industry engineers with students for professional training.
In this article, the authors aim to share their experiences and insights with peer researchers and educators regarding curriculum revamping and VLSI tapeout project design.

2. Curriculum Revamping

This work-in-progress project is targeting at developing new courses and enhancing existing courses to equip students at Electrical and Computer Engineering department with knowledge and skills on VLSI design and manufacture [9, 10]. Both undergraduate and graduate courses are involved.

2.1 VLSI Course Sequences

The core undergraduate courses involved in the project can be found in Figure 1, which illustrates the four-year computer engineering undergraduate courses.

For undergraduate courses, “Digital Logic Circuit Laboratory,” “Introduction to Digital Design,” and “Computer Organization and Design” are three required courses for undergraduate Computer Engineering degree. Previously, those courses didn't have much VLSI design content. By introducing VLSI through lectures, laboratories, and class projects, students are able to make the linkage between digital concepts to chip tapeout in three consecutive semesters. Here lists the revamped course descriptions of all the three courses. The underlined contents are either enhanced or added by the project.

ELEG 2311&2131 Logic Circuits & Lab: 1 semester hour.
Number systems and codes. Boolean algebra and logic minimization methods. Combinational and sequential design using logic gates and flip flops. Computer-aided design tools for digital design, simulation, and testing. Field Programmable Gate Array (FPGA) Devices and Verilog programming language.

ELEG 4330 Introduction to Digital Design: 3 semester hours.
The use of hardware description language and automated synthesis in design. hierarchical and modular design of digital systems. Control logic, synchronous and asynchronous sequential circuit design. Programmable logic devices and field programmable gate arrays. Circuit simulation for design verification and analysis. Timing-oriented design.

ELEG 4339 Computer Architecture & Organization: 3 semester hours.
An introduction to computer organization using assembly and machine language. Number representation, computer arithmetic, instruction sets, I/O interrupts, and programming interrupts. Projects involve detailed study and use of a specific computer hardware and software system, VLSI design project.

Freshmen Year		Sophomore Year		Junior Year		Senior Year	
Fall	Spring	Fall	Spring	Fall	Spring	Fall	Spring
ENGL1301 Freshmen Comp I	ENGL2311 Tech Writing	MATH2320 Diff Eq	ELEG2305 Network I	MATH3302 Prob. & Stat.	ELEG3302 Signals and Systems	ELEG4325 Embedded Sys. Design	ELEG4333 Computer Networks
MATH2413 Cal I	MATH2414 Cal II	PHYS2326 Univ. Physics II	ELEG2101 Elec. Cir Lab	ELEG3301 Network Theory II	ELEG3307 MicroP	ELEG4272 Senior Design I	ELEG4248 Senior Design II
ELEG1101 Intro to Eng.	ELEG1321 Prog. For CPEG II	PHYS2126 Univ. Phys. Lab II	ELEG2131 Logic Circuit Lab	ELEG4330 Digital Design	ELEG3107 MicroP Lab	POSC2305 American Gov. I	POSC2306 Texas Gov.
ELEG1102 Intro to ECE Lab	PHYS 2325 Univ. Physics I	CHEM1403 Chem for Eng.	ELEG2311 Logic Circuit	MATH2305 Discrete Math	ELEG3304 Electronics I	Technical Elective	Technical Elective
ELEG1301 Prog for CPEG I	PHYS 2125 Univ. Physics Lab I	CHEM1112 Chem Lab II	ELEG2331 Adv. Prog. & Appl	ELEG3303 Phy. Prin. of Solid State	ELEG4339 Comp. Arch. & Org.	Technical Elective	Language, Philosophy & Culture
SPCH1311 Fund. Of Speech	CVEG2304 Global Devel. Issues	ELEG2321 Data Stru. & Alg.w. Pyth	CHEG2308 Econ Analy.	HIST1301 US to 1876	HIST1302 US 1876 to Present		
			Creative Arts				

Figure 1: Computer Engineering Program Flowchart (Note: Blue marked the required courses. Green shows the technical electives, where the graduate courses can be counted as technical electives in a 5-year BS & MS program.)

Freshmen Year		Sophomore Year		Junior Year		Senior Year	
Fall	Spring	Fall	Spring	Fall	Spring	Fall	Spring
ENGL1301 Freshmen Comp I	ENGL2311 Tech Writing	MATH2320 Diff Eq	ELEG2305 Network I	MATH4317 Adv. Math for Eng.	ELEG3302 Signals and Systems	ELEG4304 Electronics II	ELEG4307 Servomech. and Control
MATH2413 Cal I	MATH2414 Cal II	PHYS2326 Univ. Physics II	ELEG2101 Elec. Cir Lab	ELEG3301 Network Theory II	ELEG3307 MicroP	ELEG4300 Comm. Theory	ELEG4248 Senior Design II
ELEG1101 Intro to Eng.	CHEM1403 Chem for Eng.	PHYS2126 Univ. Phys. Lab II	ELEG2131 Logic Circuit Lab	ELEG3303 Phy. Prin. of Solid State	ELEG3107 MicroP Lab	ELEG4301 Electromech. Field Theo I	ECE Lab Elective
ELEG1102 Intro to ECE Lab	CHEM1112 Chem Lab II	POSC2305 American Gov. I	ELEG2311 Logic Circuit	MATH2305 Prob. & Stat.	ELEG3304 Electronics I	ELEG4272 Senior Design I	Technical Elective
ELEG1304 Comp. Appl. For Eng.	PHYS 2325 Univ. Physics I	HIST1301 US to 1876	CHEG2308 Econ Analy.	HIST1302 US 1876 to Present	ELEG4101 Electronics Lab	Technical Elective	Technical Elective
SPCH1311 Fund. Of Speech	PHYS 2125 Univ. Physics Lab I	MCEG2301/ CHEG2334 Thermo	POSC2306 Texas Gov.		CVEG2304 Global Devel. Issues		Creative Arts
			Language, Philosophy & Culture				

Figure 2: Electrical Engineering Program Flowchart (Color coded same as Figure 1.)

The funded project benefits not only computer engineering students but also those in the electrical engineering program. At the undergraduate level, electrical engineering students can select the following courses as technical electives: "Computer Architecture & Organization," "Digital Design and VLSI Design." Through these courses, students will gain hands-on experience with VLSI implementation, working on practical projects assigned within the curriculum. Figure 2 presents the enhanced undergraduate electrical engineering degree plan flowchart, highlighting the integration of these advanced courses.

Graduate students in the MS and PhD programs in Electrical Engineering will also benefit from this initiative. When enrolled in the "VLSI & ULSI Design" course, they will have the opportunity to fabricate and test their designs, providing valuable hands-on experience. Figure 3(a) illustrates the prerequisite pathway leading to the undergraduate tapeout class: ELEG 4339 Computer Architecture and Organization. Figure 3 (b) highlights the prerequisite pathway leading to the graduate tapeout class: ELEG 6342 VLSI and ULSI Design, and ELEG 6391 VLSI Testing and Characterization.

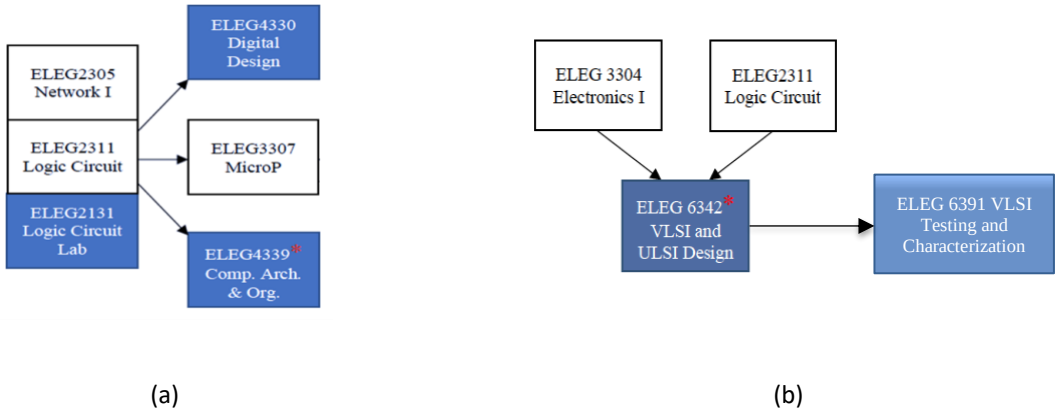


Figure 3: (a) Undergraduate courses pre-requisite link; (b) Graduate courses pre-requisite link.

2.2 Class Projects

Engineering classes rely on well-designed class projects to practice students' skills learned from the theories. The highlight of this project is the tapeout experiences introduced in classes, while there exist challenges to reach the goal. There are several reasons why chip tapeout projects are not commonly included in undergraduate courses, here list three of them:

a) **High Cost of Tools and Technology for Fabrication:**
Fabricating integrated circuits (ICs) is expensive. VLSI design and chip tapeout require specialized Electronic Design Automation (EDA) tools (e.g., Cadence [11], Synopsys, or Mentor Graphics) and access to technology libraries from foundries. Licensing costs for these tools and libraries can be high, and training students to use them effectively takes time. Tapeout projects require access to advanced semiconductor fabrication facilities (fabs), which can be cost-prohibitive for many universities.

b) **Complexity of Design:**
Tapeout projects involve the entire VLSI design process, which requires deep technical knowledge of digital design, layout, verification, and physical design flows. Undergraduates may not yet have the foundational expertise in these areas to complete a chip-level project successfully.

c) **Time Constraints and Infrastructure Limitations:**
Undergraduate programs typically operate on tight timelines (semester or quarter systems). A chip tapeout project requires multiple stages, including design, simulation, verification, and debugging, which often extend beyond a typical academic term. Setting up a chip tapeout pipeline requires a robust infrastructure, including computing resources, CAD tools, and partnerships with semiconductor fabs. Many universities lack the resources or partnerships needed to facilitate such projects at the undergraduate level.

However, with industry and department support, the authors were able to revamp the course contents and design new course materials to tackle the above obstacles. First of all, Cadence license and workstations to accommodate the users' needs were purchased by the grant, a dedicated VLSI design laboratory was established for education and research [14, 15, 16]. Second, hands-on class projects were designed to guide students learning the gist of chip design step-by-step. Multiple software simulation or EDA tools [17, 18] were introduced in the classes to prepare students ready for the chip tapeout challenge. Third, three core classes were redesigned in sequence to carry the training, starting from FPGA design with Verilog in ELEG 2311 Logic Circuit, continued with Cadence pre-tapeout for a digital counter in ELEG 4330 Digital Design, ended with tapeout project of a memory element in ELEG 4339 Computer Architecture and Organization.

2.2.1 Verilog Modules in Logic Design

The first step of VLSI design enhancement is to improve ELEG 2311 Logic Circuit class with Verilog in FPGA because FPGA design can significantly help in preparing for a Cadence tapeout project for several key reasons:

a) Verilog is a standard Hardware Description language (HDL) used for both FPGA programming and ASIC (Application-Specific Integrated Circuit) design. Students or engineers can develop and verify their designs on an FPGA using Verilog before transitioning to Cadence tools for ASIC tapeout. This ensures consistency in the design flow and minimizes errors when porting the design to an ASIC process.

b) Testing on an FPGA helps identify logical errors, timing issues, and functional bugs early in the design process, ensuring the design works correctly before moving to Cadence-based ASIC flows. Using Verilog on FPGA accelerates development and debugging without the immediate costs of fabrication. Verilog code written for FPGA design can be reused directly in the Cadence ASIC design flow with minimal modifications. FPGA tools (e.g., Xilinx Vivado, Intel Quartus) allow engineers to analyze timing, logic utilization, and area efficiency of their Verilog designs.

c) Using Verilog on FPGA prepares students or engineers for industry-standard workflows. Most VLSI design teams use Verilog for RTL (Register Transfer Level) coding before using Cadence tools for synthesis, place-and-route, and physical verification.

Thus, in the course sequence, five laboratories were developed using Verilog and FPGA platform in the ELEG2311 Logic Circuit class. The topics cover the basic logic elements design of both combinational and sequential logic designs: adder, decoder, D-Flip Flop, JK Flip Flop, and Counter [19, 20]. Intel DE10-Nano FPGA trainer and Intel Quartus Prime Lite Edition Design Software are used for all laboratory exercises. The trainers were donated from a previous university program sponsored by Intel.

All the teaching modules started with the implementation and theory behind it. Accompanied by PowerPoint slides, the modules consist of detail step-by-step procedures on setting up the software simulation and hardware testing environments. Driven by Verilog coding, both Netlist View and waveform through timing diagram are outputs to verify the analysis and synthesis results. Figure 4 through Figure 6 are images selected from the “Decoder” lab manual as samples to illustrate the teaching materials. All the materials are shared at a public accessible resource (hide for now for paper review, will include the link if selected for publication).

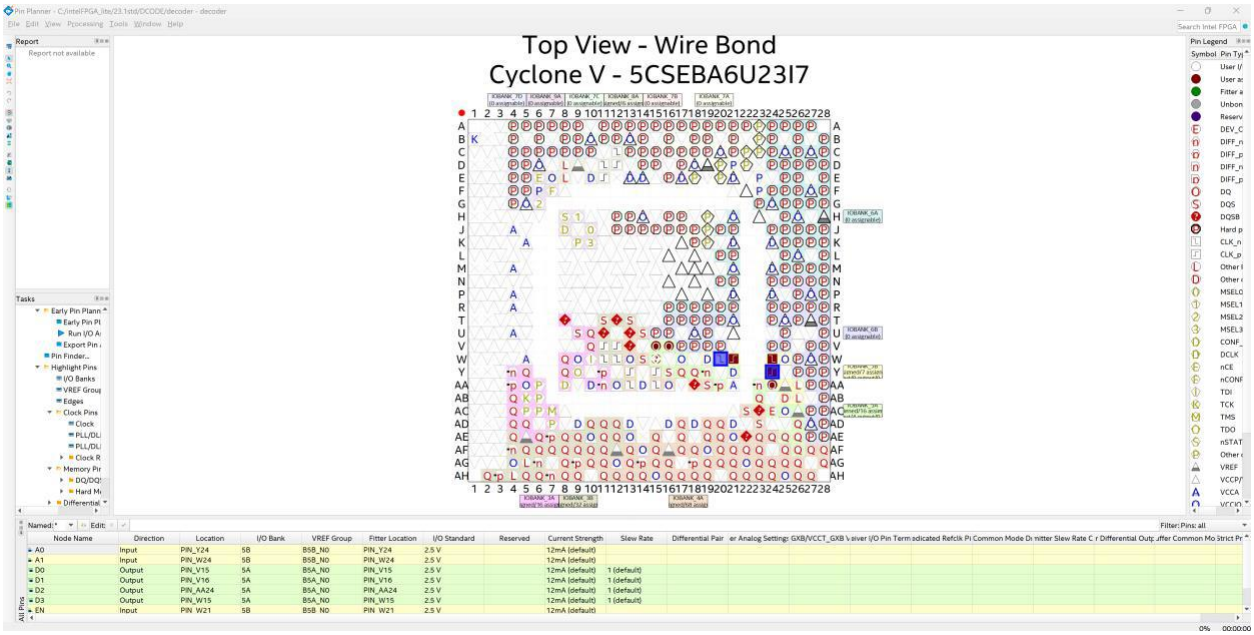


Figure 4: Pin Planner and Top View of the FPGA

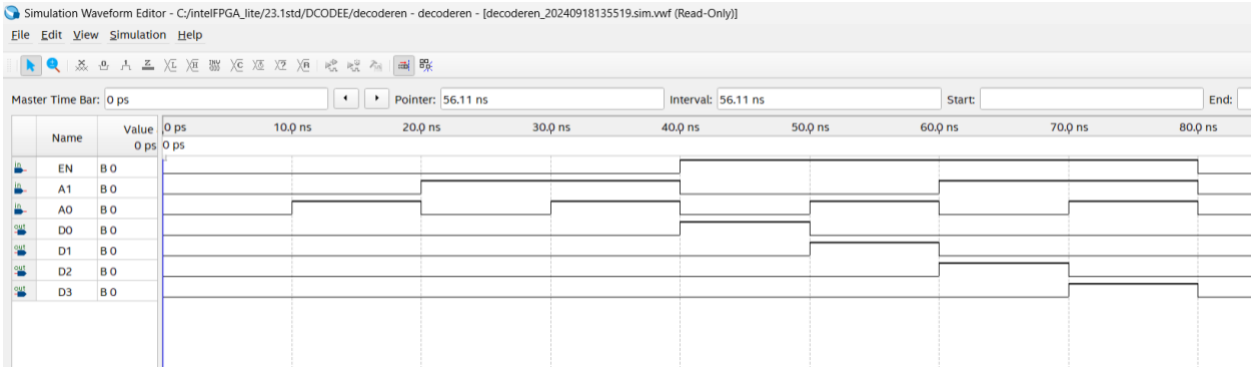


Figure 5: Timing Diagram to Verify a Decoder with Enable Circuit Design

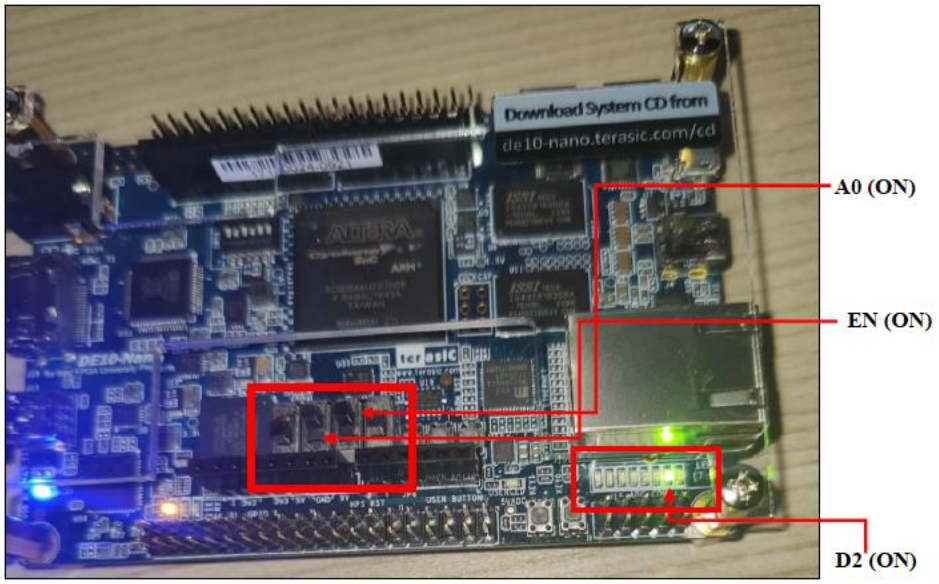


Figure 6: FPGA Trainer Output to Verify Decoder Design

After the intensive Verilog training on FPGA, students have acquired necessary skills on logic design analysis and synthesis and are confident to take the following class of Cadence tools.

2.2.2 Cadence Modules in Digital Design

After students obtain enough knowledge on hardware design through Verilog and FPGA, a pre-tapeout class was designed to prepare students familiar with Cadence tools [11]. The ELEG4330 Cadence Modules course guides students through the construction of an 8-bit counter, leveraging the RTL-to-GDSII process [21] with Cadence 6.0 EDA software [11]. This course spans the entire design cycle from the initial concept to the final physical layout. It starts with designing the RTL in Verilog, progresses through simulation, synthesis, and testing, and concludes with the physical GDSII layout. Each phase ensures the design adheres to critical specifications such as functionality, timing, and performance.

a) **Counter System Design and RTL Implementation Stage**: This foundational stage starts with students writing RTL code to define the circuit's behavior and set performance constraints. Students then simulate the design using Cadence Xcelium to verify its functionality, observing waveforms that illustrate the counting behavior (Figure 7).

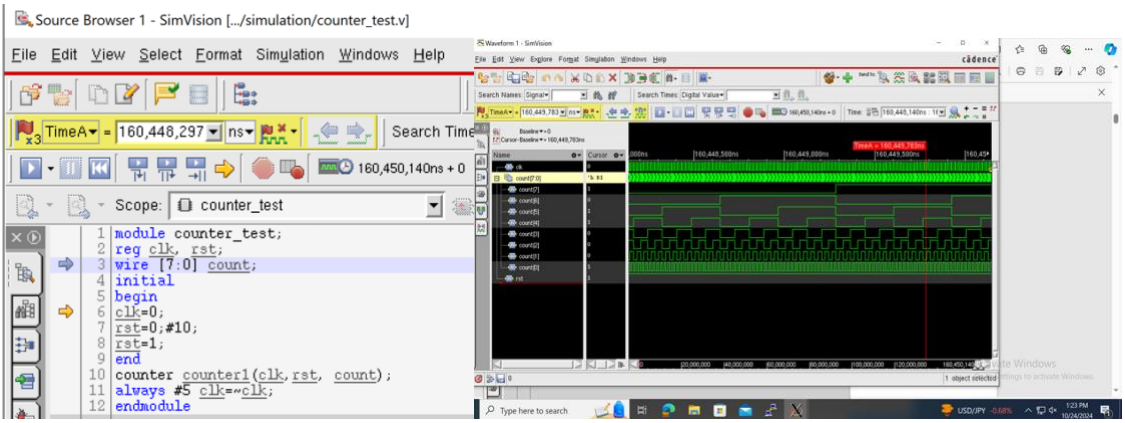


Figure 7: Verilog Code Testbench and Simulations for an 8-Bit Counter

b) **Synthesis and Gate-Level Design:** Following the simulation, the process transitions the RTL design into a gate-level netlist. During synthesis, Cadence Genus tool is employed to ensure the design meets predefined constraints like timing and area, effectively mapping the theoretical design onto actual logic gates, as shown in Figure 8.

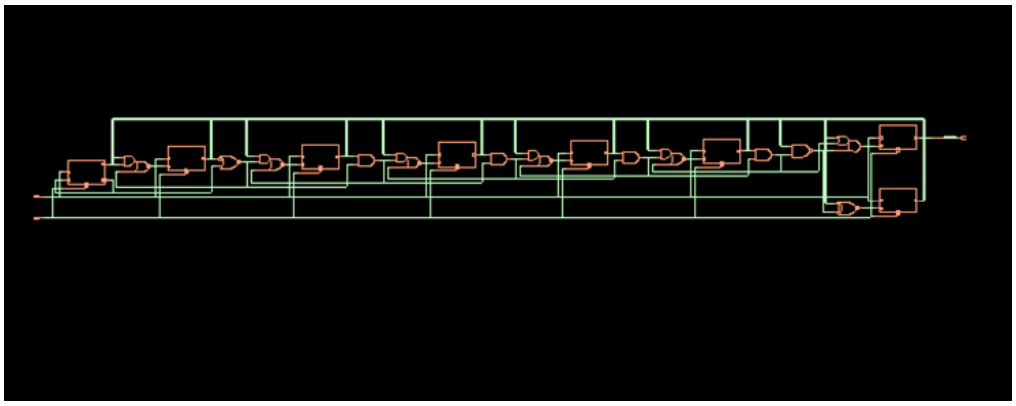


Figure 8: Gate Level Synthesis of 8-Bit Counter

c) **Test stage:** In this phase, the focus shifts to validation using the Modus Test system for automated test pattern generation (ATPG). This stage is critical for constructing and validating test models and structures to achieve full functionality coverage. It also encompasses the development of fault models and execution of scan tests, pivotal for detecting and addressing hardware manufacturing defects.

d) **The Equivalency Checking Stage:** This module immerses students in equivalence checking, a critical verification process that ensures consistency across different design stages or methodologies. The curriculum covers tool setup, initiation of checks, scripting for automation, and result analysis to confirm design consistency. Mastery of this stage is

essential for ensuring circuit reliability and performance, solidifying students' expertise in design verification.

e) **Physical Design Stage:** In this final module, students dive into the physical design process, which is critical for producing the final GDSII layout. They start by learning how to import and analyze design files, execute floorplanning, and manage pin assignments and power planning. The course then guides students through placement optimization, clock tree synthesis, and routing, complemented by detailed extraction, timing, and power analyses. Key steps such as physical verification, filler cell placement, and generating a stream file for the GDSII data are thoroughly covered, equipping students with the necessary skills to navigate the intricate stages of semiconductor design. The implementation of an 8-bit counter in physical design is illustrated in Figure 9.

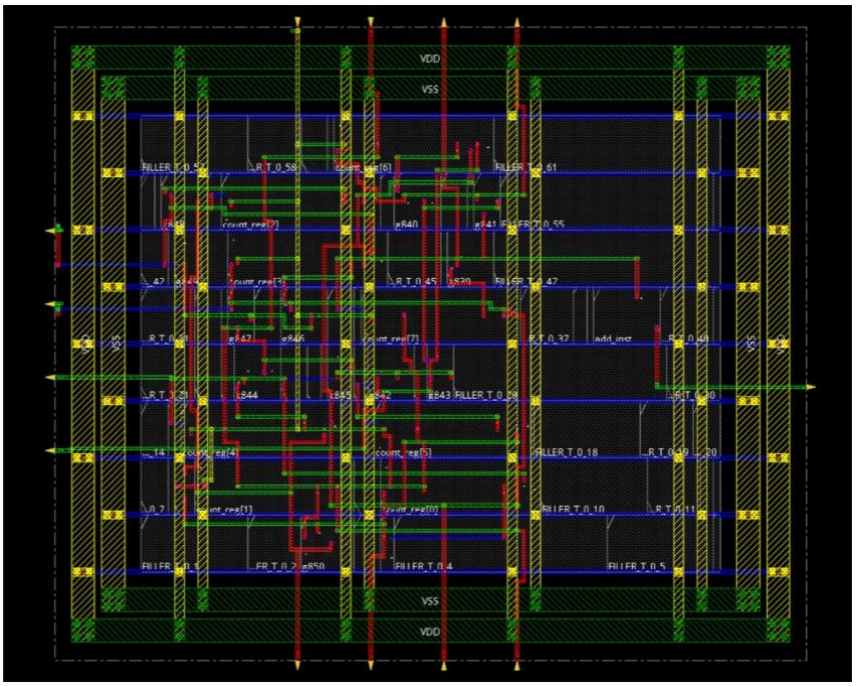


Figure 9: Physical Layout of 8-Bit Counter

Through the ELEG4330 Cadence Modules class, students master the RTL-to-GDSII flow process, an essential technique in semiconductor manufacturing that turns digital designs into functional chips. By creating an 8-bit counter, they navigate the entire design cycle from initial concept to final layout. This comprehensive training equips students with crucial skills for chip design careers, preparing them to produce manufacturable semiconductor layouts suitable for production.

2.2.3 Tapeout Modules in Computer Architecture and Organization

With the preparation from Verilog and Cadence design of previous two classes, in ELEG 4339 three individual modules (decoder, memory, and amplifier) are designed and integrated together as one chip tapeout project. The chip block diagram is illustrated in Figure 10. The decoder is a 2-to-4 decoder. It outputs 4 signals and sends them to the bit lines of each memory cell. The output signal from the memory is then amplified by an operational amplifier. The

circuit is shown in Figure 11, and the chip top view can be found in Figure 12. The design was implemented using the Cadence software platform with TSMC 180nm technology. Detailed procedural steps are documented across eight labs, which are available to the public.

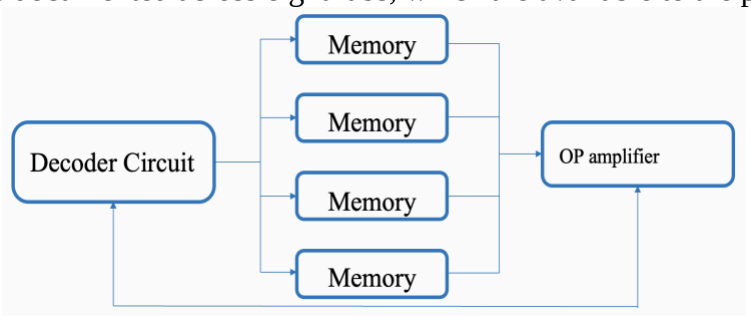


Figure 10: Tapeout Chip block : Consists of Decoder, 4 Memory Cases, and Amplifier.

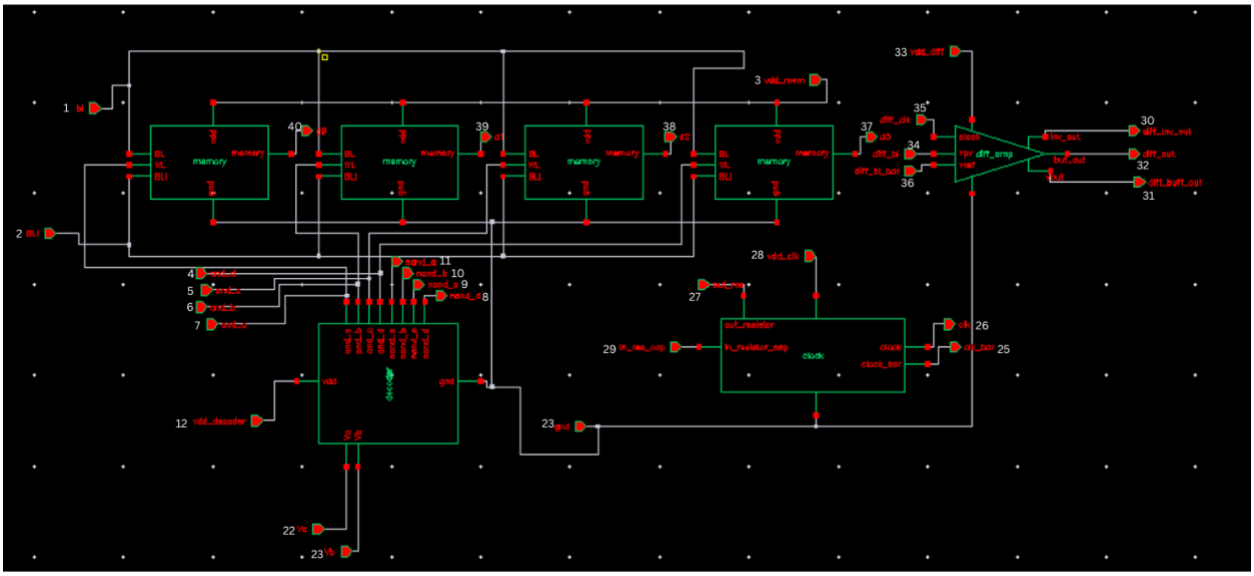


Figure 11: Circuit Layout with Pin Assignment

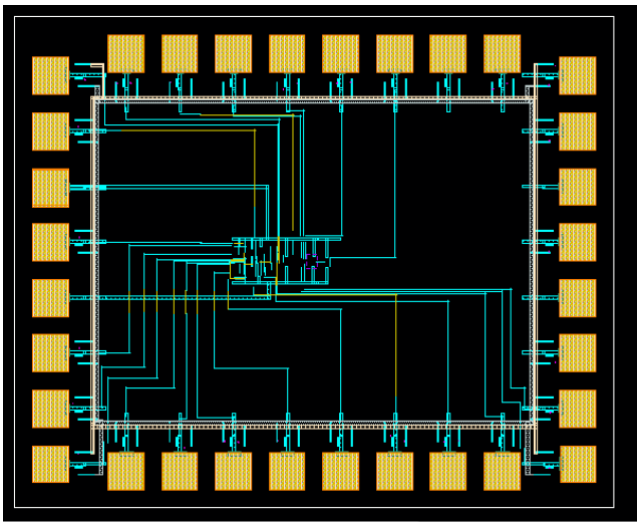


Figure 12: Tapeout Chip Circuit Top View

After sending out the design for fabrication in spring semester, the chip will come back in fall semester and be tested in the fall semester for testing in a specialized bringup class. The tapeout results and class feedback will be collected with the classes.

2.2.4 Bringup Class

After the design phase, a bringup class was specially developed to assess the tapeout chip that incorporates the three modules designed in ELEG 4339. Following the chip's fabrication by TSMC, it underwent extensive testing. ELEG 6391 VLSI Testing and Characterization is designed for the bringup task.

Students assembled all components of the custom VLSI design IC using commercially available parts. This hands-on approach not only provided invaluable experience in assembling components and conducting electrical tests but also in characterizing their properties. Given the limited availability of only five units per each of the four IC packages, totaling 20 units, careful handling was crucial.

The results from the testing of the custom TSMC-fabricated chip were promising. We successfully confirmed the functionality and electrical characteristics of several components, detailed in Figures 13 through 16:

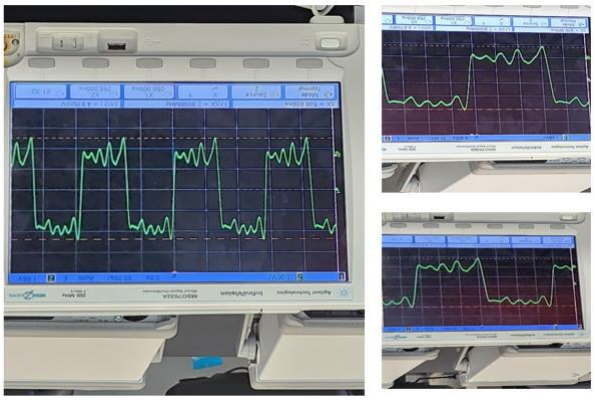


Figure 13: Clock Circuit Testing Result

The clock circuit testing result in Figure 13 demonstrated relatively consistent outputs, with rising and falling edge delays recorded at 10ns and 9ns, respectively.

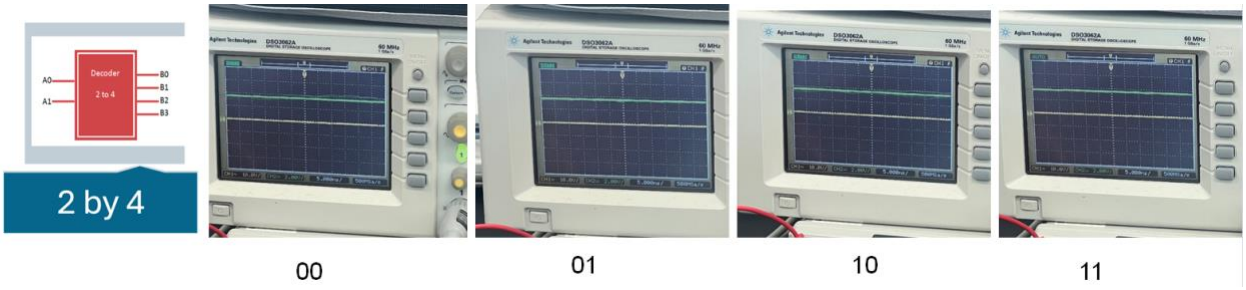
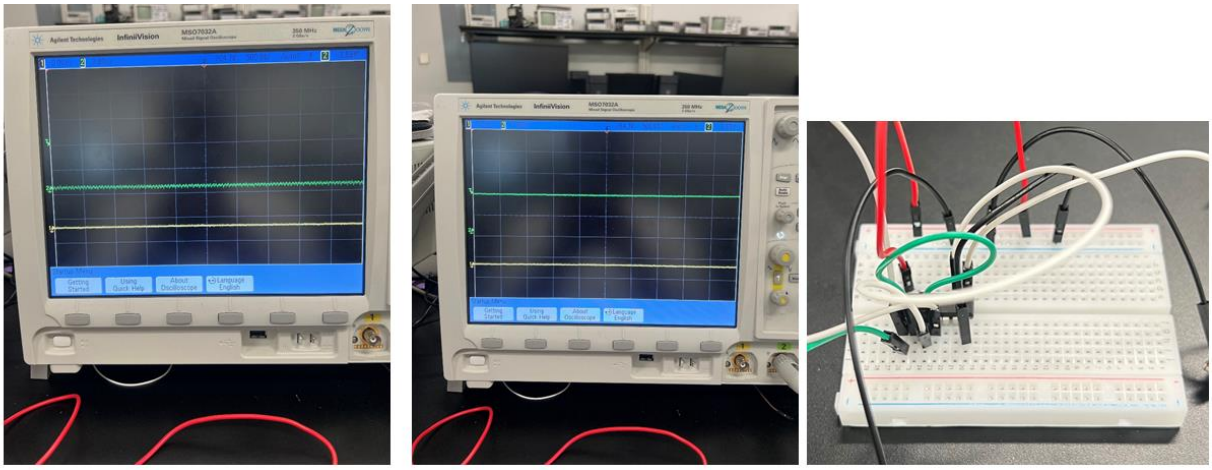


Figure 14: Decoder Testing Results

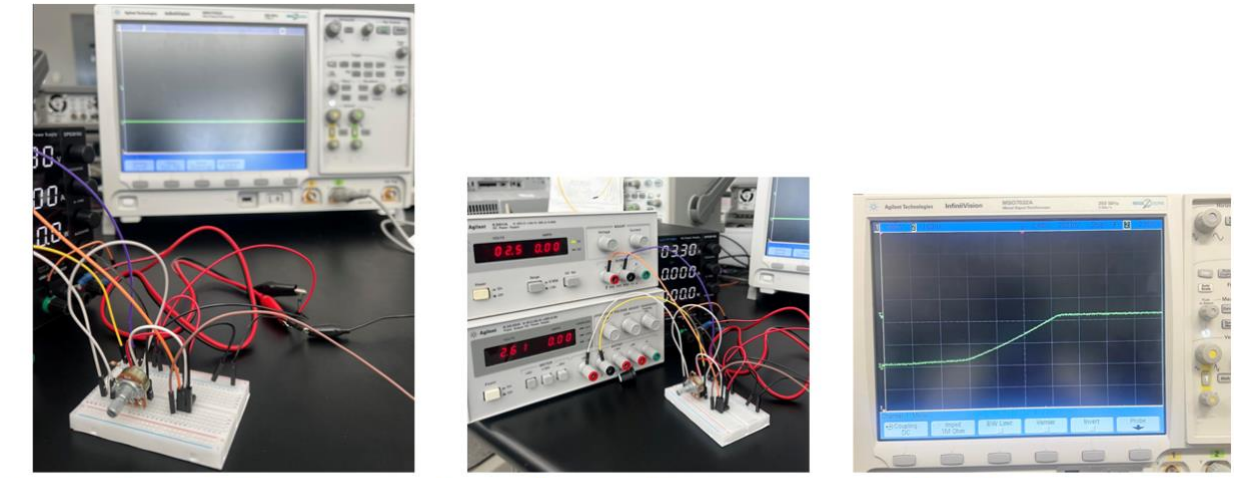
Truth table verification of the 2-to-4 decoder was conducted, yielding expected results. Figure 14 presents the outcomes from these decoder tests.



Stores a 1 and inverted output is 0 | Stores a 0 and inverted output is 1 | Breadboard setup for Memory Test

Figure 15: Memory Testing Results

Memory testing results confirmed successful functionality: storing a '1' produced an inverted output of '0', and storing a '0' resulted in an inverted output of '1', as depicted in Figure 15.



Config with Parallel Potentiometer | Source Voltage DC P/S connected to +ve terminal in a voltage divider configuration | State Change Time = 65us

Figure 16: Differential Amplifier Testing Configuration Example and Results

We conducted several configurations of differential amplifier tests, including setups with and without a potentiometer. Figure 16 presents an example of the differential amplifier tests utilizing a potentiometer configuration, where students successfully recorded the state change times.

With these positive outcomes from the custom TSMC-fabricated chip, confirming the functionality and electrical characteristics of its components, we are well-positioned to advance to the next phase: incorporating this experience into our digital design chip tapeout and fabrication testing processes.

3. Class Surveys and Analysis

Class surveys were conducted in two formats: a structured questionnaire or a class learning summary report to collect comprehensive feedback from students.

3.1 Questionnaire Survey

For the ELEG 4330 Digital Design course, surveys were collected both before (pre-survey) and after (post-survey) the course to assess its impact, identify strengths, and pinpoint areas for improvement. We employed a five-point scale ranging from 'no experience' to 'extensive experience' to measure proficiency across various key skills. The questions focused on critical areas of digital design, as listed in Table 1.

Table 1: Pre and Post Survey Questions for Course Involved

No.	Survey Questions
1	What is your current level of familiarity with the RTL-to-GDSII design flow?
2	What is your current experience level with Verilog or VHDL?
3	What is your experience level with the Xcelium™ Simulator tool?
4	What is your experience level with the IMC code coverage analysis tool?
5	How familiar are you with floor planning, placement, and routing?

The outcomes of these surveys were graphically represented to show a clear comparison of the skill levels before and after the course. Figure 17 illustrates these changes, demonstrating significant student advancements in each area.

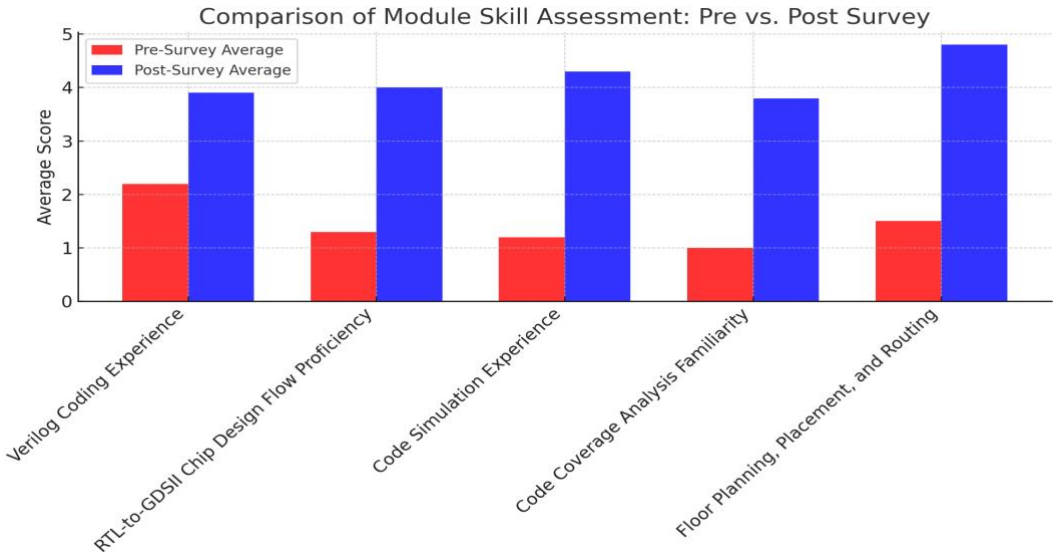


Figure 17: Comparisons of Key Skills Reflected on the Survey Data Before and After the Cadence Modules class.

The above pre- and post-survey comparisons indicate significant gains in crucial technical skills through the Cadence Modules course. It is observed that there were notable improvements in RTL-to-GDSII chip design [21] and essential chip tape-out processes, including floor planning, placement, and routing—skills crucial for the semiconductor industry. These substantial enhancements not only show the students' improved abilities but also emphasize the course's role in equipping them for specific industry challenges.

3.2 Learning Summary Survey

In addition to questionnaires, feedback was also collected through written class learning summaries. After the bring-up class, students reported significant gains in practical skills:

- **Accurate Measurement:** Students learned to measure sheet resistance accurately using a 4-probe setup.
- **Defect Identification:** They gained the ability to identify manufacturing defects through resistance measurements in VDD and GND metal setups.
- **Voltage Drop Minimization:** They developed skills in minimizing voltage drops using thick VDD and GND lines.
- **Timing and Frequency Analysis:** Students improved their ability to analyze timing delays and frequency responses using logic ICs and op-amps.
- **FPGA Programming:** They gained experience in programming FPGA boards for specific applications like solar panel diagnostics.
- **Automated Testing and Debugging:** They learned to apply automated testing techniques and debug various design modules.

This dual approach to feedback collection has substantially enhanced our understanding of the educational impact and will inform future curriculum development to align more closely with educational and industry-specific objectives.

4. Conclusion

This ongoing project aims to strengthen the Computer Engineering program at PVAMU by integrating advanced VLSI concepts into the curriculum. Over the past two years, a sequence of courses has been revamped to include VLSI content. The program introduces Verilog training in sophomore-level courses, transitioning to Cadence tools in junior-level courses. Additionally, tapeout projects have been successfully incorporated as final project assignments in both undergraduate and graduate courses.

Specifically, computer engineering students receive training in VLSI implementation through courses like *Computer Architecture* and *Digital Design*. Future phases of the project will include more extensive class surveys to guide further analysis and development. The hands-on experience gained through the program equips students with valuable skills, enhancing their employability in high-tech industries.

Moreover, this initiative has significantly enriched both undergraduate and graduate curricula at a minority-serving institution, contributing to the development of a more diverse workforce. The project team is also working to further enhance the curriculum by grouping the revamped courses into a certificate program focused on computer hardware and VLSI design. At the meantime,

faculty and graduate teaching assistants training will be prioritized for future long-term funding to sustain the educational accomplishments.

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