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Assessing the alignment of examinations with course intended learning outcomes in an electrical circuits course

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Abstract

High-stakes final examinations are defined as assessments that significantly impact student progression, typically accounting for 50% or more of the overall course assessment weight, or explicitly requiring students to achieve a passing grade to successfully complete the course, known as a ‘hurdle’ requirement. However, several critical issues arise from the use of these examinations, particularly regarding their validation, focus, and alignment with the course’s educational objectives.

One major concern is that high-stakes exams often lack rigorous validation processes to ensure they accurately measure student abilities. This absence of validation can undermine the credibility of the results, meaning that these exams may not genuinely reflect a student's knowledge or skills. Additionally, these examinations frequently concentrate on specific content areas, which may not encompass the full range of skills and knowledge students are expected to acquire. This narrow focus can create a disconnect between what is taught and what is assessed, ultimately compromising the educational goals of the course.

Despite these drawbacks, high-stakes final examinations remain prevalent in universities due to their perceived efficiency in assessing large groups of students in a standardised manner. While universities mandate that assessment tasks align with intended learning outcomes, the construction of these exams often occurs with a more holistic, and less detailed alignment, leading to inconsistencies.

This paper investigates the alignment between course intended learning outcomes, indicative content, and final examination questions in an electrical circuits course with approximately 100 students. The course included a 60% final ‘hurdle’ exam, qualifying it as a high-stakes assessment. The examination paper questions were analysed for their coverage of the course intended learning outcomes, indicative content and how these related to the distribution of marks across questions. Furthermore, questions were categorised using Bloom’s taxonomy to assess cognitive levels in relation to those implied in the course intended learning outcomes.

The analysis revealed that an overall score from an examination does not necessarily accurately indicate a student’s knowledge or ability across the course intended learning outcomes or indicative content. The paper provides recommendations for engineering educators who utilise high-stakes final examinations, emphasising methods to ensure alignment with intended learning outcomes and providing students with comprehensive feedback on their performance relative to these outcomes, beyond solely their final grades.

Introduction

High-stakes final examinations, which comprise a significant weighting (typically equal or greater than 50%) of the total assessment of a course, are a common method of assessment in education, largely due to their efficiency at administering at scale. However, the implementation of these examinations brings several important concerns to light, revealing that they may not be an accurate or effective measure of a student's knowledge and/or capabilities [1]. High-stakes exams often focus on a narrow range of knowledge and skills, primarily emphasizing rote memorization and recall rather than deeper understanding and application of concepts. This approach can lead to superficial learning, where students prioritize short-term retention of information over long-term comprehension [2]. Furthermore, in electrical engineering, where practical application and problem-solving are crucial, such assessments fail to capture a student's ability to integrate knowledge into real-world scenarios [3].

High-stakes examinations tend to activate extrinsic motivation - students focus on achieving high grades rather than fostering a genuine interest in learning [4]. This shift can diminish intrinsic motivation, which is essential for deep learning and mastery of complex engineering concepts. Consequently, students may resort to cramming or surface learning strategies that do not promote a thorough understanding of the subject matter [5].

Due to their summative nature, final examinations typically do not provide opportunities for feedback or iterative learning processes. In engineering education, where problem-solving and critical thinking are vital, a small amount of formative assessment limits students' ability to learn from their mistakes and improve over time. Without mechanisms for feedback, students miss out on valuable insights that could enhance their understanding and application of engineering principles, particularly when this knowledge is relied upon in future courses.

In paper, we report on a study of the alignment between course intended learning outcomes, indicative content, and final examination questions in an electrical circuits course with approximately 100 students. Examination paper questions were analyzed for their coverage of the course intended learning outcomes and indicative content, as well as how these related to the distribution of marks across questions. Questions were further categorized using Bloom's taxonomy to assess cognitive levels in relation to those implied in the course intended learning outcomes. The analysis highlights some of the shortcomings associated with high-stakes final exams acting as a broad indicator of a student's knowledge or ability across the course intended learning outcomes or indicative content.

The paper concludes by offering recommendations for engineering educators who utilize high-stakes final examinations. These recommendations emphasize methods to ensure alignment with intended learning outcomes and stress the importance of providing students with comprehensive feedback on their performance relative to these outcomes, beyond solely their final grades.

Background and Context

Scaffolding learning [6] is an approach that helps students build their understanding of complex electrical circuits progressively by breaking them down into more manageable parts; moving from basic concepts to more complex applications both within a course and over the duration of their degree [7]. University degrees are normally highly structured to support scaffolded learning through prerequisite chains of courses, minimum GPA thresholds or hurdle requirements. For example, students typically learn basic physics before moving on to elementary circuit principles such as KVL, KCL for DC circuits that form the basis of most circuit solving techniques such as Node Voltage or Mesh Current Analysis. After this, AC analysis can be introduced, usually through phasors, and then more complex frequency-domain analysis as students' knowledge grows. This knowledge must be developed over a number of courses over several years, requiring students to take solid foundations from each course and build upon them in the next one. This approach relies on the assessment regime ensuring that students have the necessary prerequisite knowledge to successfully build upon in subsequent courses, and often high-stakes exams are employed as form of 'gatekeeping' mechanism to guarantee this.

There are methods to improve the reliability and validity of exam questions, for example having independent subject-matter experts review them, which can take significant time and might require historical data from past exams, or through metrics such as discrimination levels on single- or multi-tiered multiple-choice questions [8], which are not suitable for long answer-type questions. Without robust validation procedures, doubts can be cast on the exams' ability to genuinely assess a student's knowledge and skills. For example, a student that passes an exam that tests fundamental circuit principles may have done so by excelling in one area (DC circuits), while performing poorly in another (AC circuits) such that the overall exam mark is still a passing grade. This would be problematic for any subsequent courses that rely on the student's AC circuits knowledge, yet their lack of knowledge would be indistinguishable from the pass grade they achieved overall for the exam and the course as a whole. Moreover, high-stakes final exams often have a tendency to focus on narrow content areas, potentially overlooking the broader spectrum of competencies and knowledge that students are expected to develop throughout their studies. This limited scope can create a misalignment between the curriculum taught in classrooms and the material evaluated in these exams. Consequently, this disconnect may undermine the overarching educational objectives of the course or program.

The electrical circuits course that is the subject of this study is at the third-year of an undergraduate mechatronics degree and covers concepts from both analog and digital electronics. The course intended learning outcomes (ILOs) describe the abilities that students should have developed through completing the course. On successful completion of the course, a student is expected to be able to:

1. Model and analyse the linear time-invariant behaviour of electrical and electronic systems, in both the time and frequency domain (*)

2. Design, construct and test passive and active electrical networks that achieve specified linear time-invariant behaviour (*)
3. Use software tools to simulate the behaviour of linear electrical networks
4. Apply fundamental concepts and tools in the analysis and design of combinational and sequential logic systems, with an appreciation for the role and limitations of important digital abstractions (*)
5. Configure and test digital hardware development platforms in the laboratory

ILOs marked with an asterisk (*) are outcomes that are assessed on an end of semester, three-hour written final examination, which comprises 60% of the final assessment of the course. The examination is also a hurdle requirement, in that students must pass the examination in order to pass the course, and therefore can be considered a 'high-stakes' assessment. Students are not given any further information about the breakdown of the exam marks with respect to these ILOs and thus could reasonably assume that they are all equally important in being met. Furthermore, students are not given solutions or detailed feedback on their exam results, other than having the opportunity to view their completed papers after results have been released.

As is typical for course outlines, the course ILOs are relatively vague and are therefore supplemented with a list of 'indicative content' covered in the course:

> Analog systems - time-domain differential equation models of RLC networks, initial conditions, transient response, transfer functions, frequency response, passive filters, impedance functions, two-port networks and dependent sources and matrix circuit representations, op-amp models.
>
> Digital systems – encoding information and digital data processing, CMOS realisation of basic logic gates, timing contracts, acyclic networks, switching algebra, combinational logic synthesis, cyclic networks and memory, finite-state machines, metastability, synchronous timing and synchronization, data-processing paths, control logic and stored-program machines.

To limit the scope of this study, only the analog section of the course will be considered, primarily due to the effort required in categorizing and reassessing all student exam papers. Also, the course sits between tightly scaffolded prerequisite and subsequent analog electronics courses, so the analysis could provide insight into the students' success in the future based on these exam results. This research was approved under Human Ethics Protocol 29248.

Methodology

The analog section of the exam comprised of five questions, totaling 86 marks. Some questions were also split into smaller sub-questions related to the overall theme/topic of the question. Each

question was assessed using a revision of Bloom's taxonomy in the cognitive domain [9] to gauge the cognitive processes that students would use with their knowledge:

- Remember
- Understand
- Apply
- Analyze
- Evaluate
- Create

Marks associated per (sub)-question can be associated with a cognitive level to yield an overall measure of the composition of the exam across each level.

A list of key concepts, drawn from the indicative content in the course and with reference to some identified threshold concepts in analog electronics [10], was composed and is shown in Table 1.

Table 1: Analog electronics concepts in the course (as assessed on examination)

Time-domain circuit models	Circuit solving	General frequency response
Lumped circuit abstraction	Transfer functions	Designing / drawing circuits
Time-frequency domain transformations	Passive filters	Linear algebra
		Units, other minor details

The marks for each question were projected onto these – for example, if two marks in a question were allocated for performing mathematical, manipulation of circuit equations, this would be classified as two marks under 'Linear Algebra'. Each student paper was reassessed according to this categorization, noting that the final mark for the exam would be the same as the original marking scheme was simply being reclassified and used as an 'overall performance' reference.

Results

Ninety-two students sat the final exam and made a reasonable attempt at completing the paper. Figure 1 shows a histogram of the results of the analog section of the exam. The mean score was 47 out of a possible 86 marks (54.7%), with a standard deviation of 16.5. As there is a reasonable

proportion of students around the pass level, it is highly likely that some students are progressing with only a partial understanding of important material.

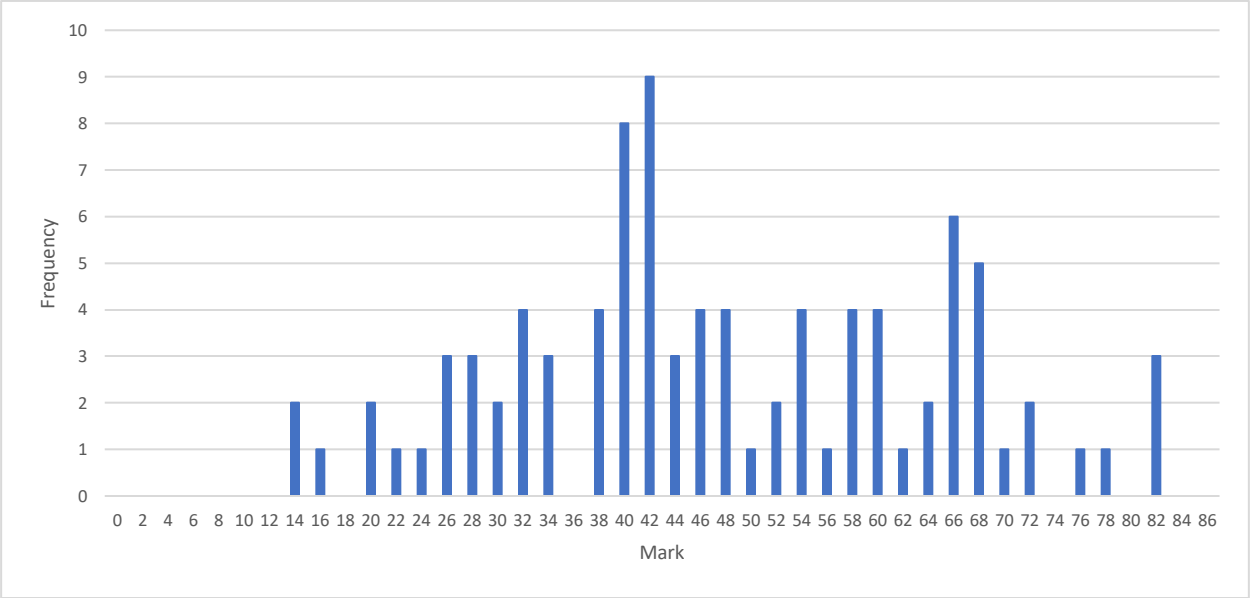

Figure 1: Histogram of final exam marks

To highlight this, the distribution of marks for Questions 1-3 are shown in Figure 2. From this, it can be seen that student performance is not uniform across questions and instead likely depends on the question content and its cognitive level. This might indicate that some students are passing the examination hurdle overall while performing below a pass level on particular topic areas.

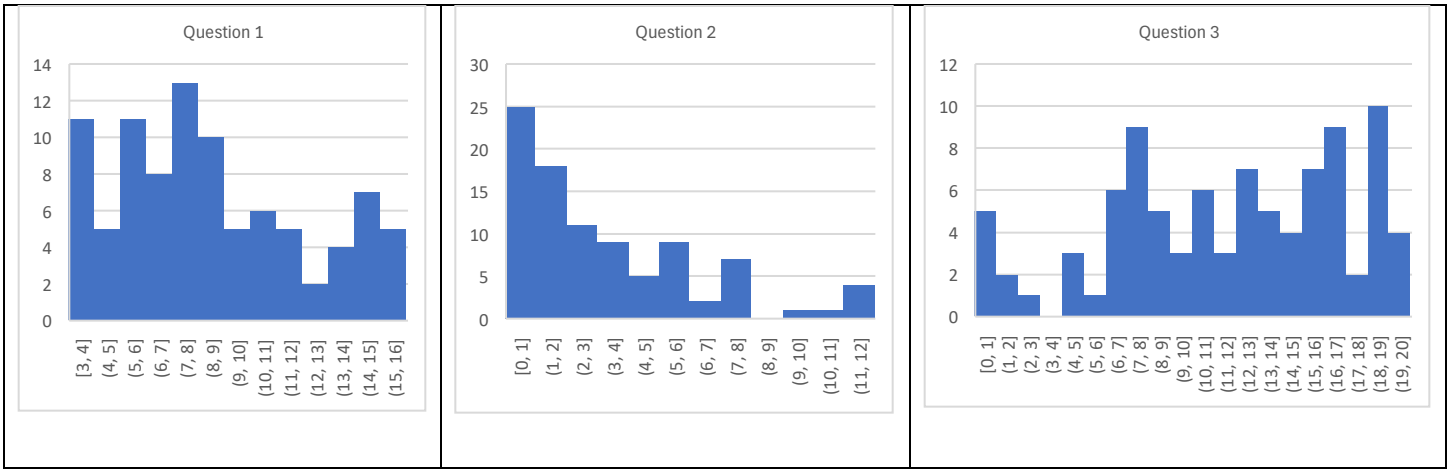

Figure 2: Histograms of exam marks for selected questions (Q1-Q3)

Table 2 shows a breakdown of the marks as per the concepts identified in Table 1 and the average score per concept.

Table 2: Breakdown of marks versus course concepts

Concept	Marks available	Percentage of total	Average score
Time-domain circuit models	4	5%	30.7%
Lumped circuit abstraction	6	7%	56.1%
Time-frequency domain transformations	5	6%	56.0%
Circuit solving	22	26%	57.1%
Transfer functions	3	3%	57.5%
Passive filters	5	6%	60.5%
General frequency response	19	22%	61.6%
Designing / drawing circuits	6	7%	59.1%
Linear algebra	12	14%	39.2%
Units, other minor details	4	5%	58.3%

It is apparent that broadly students scored relatively poorly on linear algebra and time-domain circuit models concepts. With these concepts comprising almost 20% of the total exam mark, it can be easily understood why the average score is 54.7%, even when students are on average scoring close to or above 60% for other concepts.

However, this does not tell the full story: Table 3 shows the average scores across concepts for the fraction of students that scored between 40% and 60% overall on the examination, compared to the student cohort averages. These results correspond to students who are just passing or just failing the subject (note that students who fall short of the hurdle requirement may potentially be given an opportunity to pass the subject under certain circumstances).

Of note is that there are significant differences in the scores for linear algebra and time-domain circuit models (~12% and ~9%, respectively), indicating that students who are struggling with such elementary concepts could be progressing to subsequent courses with an even weaker or inadequate understanding in these concepts. This would likely lead to issues as these courses assume that students that have passed the course have met all of its learning outcomes and have adequate knowledge of the indicative content. Interestingly, general frequency response concepts remain the same as the average for the entire cohort, which also was the strongest performing concept overall.

Table 3: Average concept scores for students close to passing grade

Concept	Average score for cohort	Average score for students with between 40% and 60% overall exam mark
Time-domain circuit models	30.7%	18.6%
Lumped circuit abstraction	56.1%	49.3%
Time-frequency domain transformations	56.0%	52.8%
Circuit solving	57.1%	50.8%
Transfer functions	57.5%	53.1%
Passive filters	60.5%	53.8%
General frequency response	61.6%	61.6%
Designing / drawing circuits	59.1%	52.3%
Linear algebra	39.2%	30.0%
Units, other minor details	58.3%	53.3%

These data raise an interesting question and core to some of the issues associated with high-stakes final exams – are there students who are overall passing the examination (in some cases comfortably) but who are not achieving a passing grade on a particular concept? An analysis of student results found that there were 34 such cases; some students obtained final exam scores above 75% while not achieving passing grades for concepts such as time-frequency domain transformations, linear algebra, or transfer functions (or in some cases, combinations of multiple of the three).

A question that may arise with the results presented above is whether students are being assessed at the appropriate level in the taxonomy. Table 4 shows the distribution of the marks according to Bloom's taxonomy.

Table 4: Breakdown of marks according to Bloom's taxonomy (total of 86 marks)

Level	Marks	Percentage of exam marks
Remember	-	-
Understand	1	1.2%
Apply	52	60.5%
Analyze	27	31.4%
Evaluate	3	3.5%
Create	3	3.5%

It can be seen from these results that over 90% of the exam marks come from the Apply and Analyze levels of the taxonomy, which is not unexpected as (a) testing lower levels of the taxonomy such as Remember and Understand on an exam is not considered good assessment practice as it encourages rote learning; and (b) Evaluate and Create levels are typically assessed through practical project activities during semester. Examining the course ILOs reveals that two of the three ILOs map to the analog section of the final examination – one is at the 'Apply' level and the other at the 'Analyze' level, which implies the examination is broadly in alignment.

A plot of all students' scores on the Analysis scale versus the Application scale is shown in Figure 3.

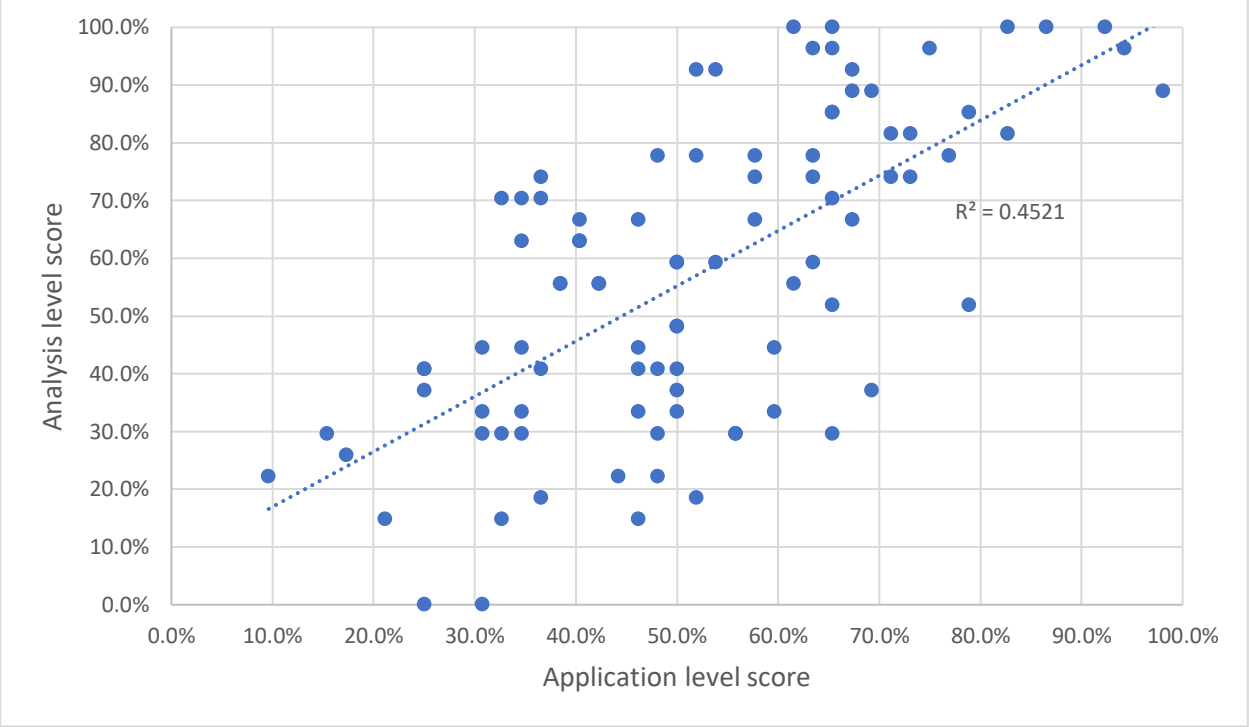

Figure 3: Analysis score versus Application score

There exists a statistically significant, moderate positive correlation ($r = 0.672$, $p < .001$) between the Analysis score and the Application score. If Bloom's taxonomy is interpreted as a

hierarchical structure, one could imagine that students who are proficient at the Analysis level would also be proficient at the (lower) Application level. There are, though, cases visible in Figure 3 where students did much better on the Analysis questions than the Application ones, and vice versa, indicating that the performance at a cognitive level is likely more complex and related to particular concept areas.

Discussion

The results indicate that the final examination is aligned with the appropriate ILOs at the correct levels of Bloom's taxonomy. This is an important analysis to perform for engineering educators when faced with using high-stakes final exams to counter criticism with regards to encouraging rote learning if questions rely too much on the Remember or Understand levels of the taxonomy. However, there are some limitations to the study. As the ILOs are written in a vague manner, it was not meaningful in this case to map them to specific exam questions. For example, ILO 1 mentions circuit analysis in both the time and frequency domains, concepts which had clearly different results when considered separately. The analysis performed in this study has highlighted that such compound ILOs could be broken out into more distinct sub-ILOs to ensure more accurate mapping and better alignment with the examination paper, in addition to balancing the potential detriment of having too many ILOs.

It was determined that it is possible for students to pass the exam (and consequently the course) without demonstrating sufficient competency in certain indicative content areas. This demonstrates that a final exam with a hurdle requirement does not automatically ensure students have passable knowledge across each of the course concepts. Note that in this case some concepts did not have large percentages associated with them, so grading could be considered coarse, and potentially prone to the effects of students making mistakes under exam pressure. Ensuring equal balance across indicative content when constructing an examination paper would alleviate this to an extent but would be difficult to achieve in practice. It is therefore recommended that educators write their papers as they normally do and use the taxonomy and content mappings as part of a review process. This would then inform small adjustments to the paper and/or marking scheme if there are disproportionalities in certain areas.

Due to final examinations being a summative assessment, detailed feedback is not normally provided to students. However, if the mapping procedure (either to course ILOs or to course concepts) as outlined in this paper is performed during the marking process, students could be provided with more feedback on their performance across these dimensions. This could give them better insights into their knowledge and highlight areas they might need to work on as they head into subsequent courses that rely on this knowledge.

Conclusion

A critical examination of the alignment between intended learning outcomes, course content, and a high-stakes final examination in an electrical circuits course involving approximately 100 students was performed. Analyzing exam questions through the lens of Bloom's taxonomy and

mapping their cognitive levels against the course's intended learning outcomes uncovered several insights, including that an overall examination score does not necessarily provide an accurate representation of a student's comprehensive knowledge or abilities across different areas of course content. To reduce the possibility of misalignment, it is recommended that educators take a holistic view of their examination papers through a similar process to ensure that questions genuinely reflect course objectives.

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