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BOARD # 297: RET: Acquisition and Retainment of Semiconductor Knowledge among K-12 STEM Teachers

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I am a Professor at Oklahoma State University interested in pushing the frontiers of computation within digital logic for general-purpose and application-specific computer architectures. I have interests in logic design for high-speed and low-power arithmetic, VLSI, FPGA, memory architectures, divide and square root implementations, computer architectures, cryptographic implementations, and graphics applications.

I have also developed several design flows for use with Electronic Design Automation (EDA) tools, including the FreePDK with my colleagues Rhett Davis from NC State University and those at the Semiconductor Research Corporation (SRC), several Cadence Design Systems (CDS) flows including the GPDK and MOSIS flows for use with CDS, National Science Foundation-funded OpenRAM, and Mentor Graphics and Synopsys EDA flows. I have also developed design flows for Google, Skywater Technology, IBM, trusted foundry, and the US Air Force. I am committed to use my experience to help others learn these tools and help develop them to further research endeavors for everyone involved.

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John Hu received his B.S. in Electronics and Information Engineering from Beihang University, Beijing, China, in 2006 and his M.S. and Ph.D. in electrical and computer engineering from the Ohio State University, Columbus, OH, in 2007 and 2010, respectively. He worked as an analog IC designer at Texas Instruments, Dallas, between 2011 and 2012. He was a Member of Technical Staff, IC Design at Maxim Integrated, San Diego, CA, between 2012 and 2016, and a Staff Engineer at Qualcomm, Tempe, AZ, between 2016 and 2019. In 2019, he joined the School of Electrical and Computer Engineering at Oklahoma State University, where he is currently an assistant professor and Jack H. Graham Endowed Fellow of Engineering. His research interests include power management IC design, hardware security, and energy-efficient computing.

RET: Acquisition and Retainment of Semiconductor Knowledge among K-12 STEM Teachers

Introduction

The semiconductor industry has played a vital role in driving economic growth and technological advancement. As an essential component of electronic devices, semiconductors power a wide range of applications, including computers, cellphones, communication systems, healthcare, transportation, and countless other sectors [1], [2]. Developing a skilled semiconductor workforce is essential, and K-14 educators are pivotal in motivating and preparing students for careers in microelectronics [3]. However, the complexity of engineering concepts, such as those related to semiconductors, poses significant challenges for teachers without specialized training. Additionally, teachers face curricular limitations in incorporating semiconductor education due to constraints imposed by state testing [4]. To address this gap, the National Science Foundation (NSF) Research Experiences for Teachers (RET) program, known as Chip-RET, was established at Oklahoma State University [5]. This first-of-its-kind program in the United States provides hands-on research experiences and professional development tailored to semiconductor education, equipping STEM teachers with the knowledge and tools to motivate the next generation of semiconductor professionals.

In the first two years of this program, Chip-RET has demonstrated measurable success in enhancing teachers' content knowledge and fostering a strong sense of community through its cohort-based structure. Participants benefited from immersive research experiences, the pSEMI and ZeroToASIC speaker series, and mentorship from faculty, which connected them to industry contexts and enabled them to bring real-world applications into their classrooms. Building on this foundation, program facilitators are committed to offering continued support, including shared resource folders, a LinkedIn group for ongoing communication, and extended guidance for chip design projects. Future initiatives will expand outreach to attract a more diverse cohort of teachers and involve state-level stakeholders in developing new semiconductor education opportunities for our students.

Methodology

Measuring teachers' progress in acquiring semiconductor knowledge presents unique challenges. Unlike other aspects of teacher evaluation, such as their alignment with Design, Engineering, and Technology (DET) frameworks [6], there is no standardized survey or questionnaire designed to assess the semiconductor content knowledge of the average adult. To address this gap, this study employed a mixed-methods approach, including pre/post surveys, mid-program feedback forms, and semi-structured interviews. A custom Semiconductor Knowledge and Literacy Test (SKLT), with content validity evidence collected through industry experts [7], was used to assess changes in teacher content knowledge. Statistical analyses, including Wilcoxon Rank-Sum test, were conducted to evaluate the significance of observed changes.

Results

The data from the first two years of the program highlights significant gains in teacher content knowledge and positive impacts on their teaching practices. In Year One, the cohort of ten teachers demonstrated an increase in their mean percentage of correct responses to the SKLT test, from 39% to 65% pre- and post-RET. A follow-up Wilcoxon Rank-Sum Test underscored the significance of this difference, with a W-value of 3 and a p-value of 0.001. Moreover, a repeat measure of the SKLT test nine months after the Chip-RET training (post-9 months) showed a mean percentage of correct responses of 55%, suggesting that participants retained much of their knowledge gained nearly one year after the training. A Wilcoxon Rank-Sum Test from pre- to post-9 months showed a W-value of 12 and a p-value of 0.007, as shown in Table 1, further confirming the gain despite some loss of knowledge over the nine-month period. It is worth noting that our RET program was designed to be independent of the SKLT test to discourage and avoid rote instruction [7].

Similarly, another cohort of ten teachers exhibited a comparable trend in Year Two. Pre-assessment scores rose from 48% to 69% post-RET, with a significant p-value of 0.009. Although the post-9 months data for Year Two is not yet available, the preliminary findings align with the Year One results, suggesting the program's consistent effectiveness in enhancing teacher knowledge of semiconductor concepts. Together, the data from both years underscores the program's impact in equipping teachers with the skills necessary to integrate semiconductor education into their classrooms.

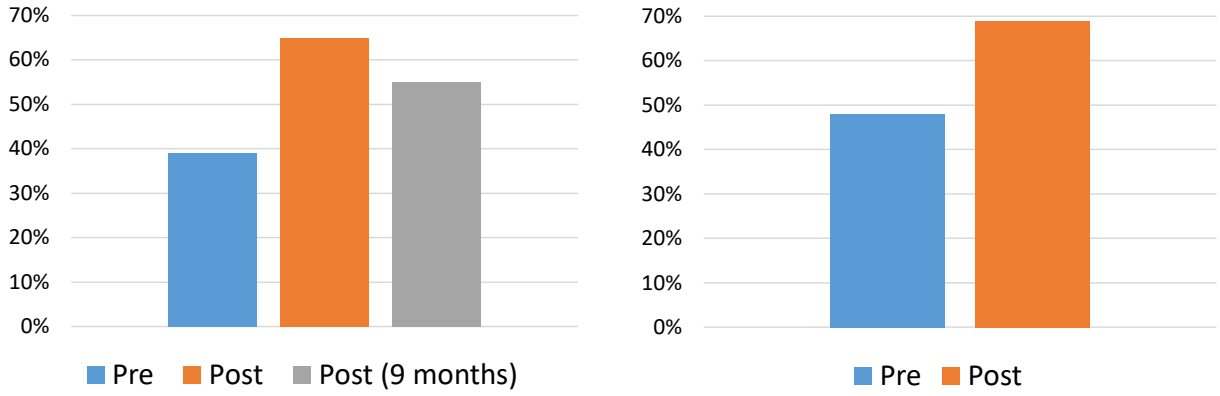

Figure 1: Mean percent change from pre to post assessment. (a): Year One, (b): Year Two

Challenges and Recommendations

Based on data collected throughout the implementation of the RET program, key areas for improvement have been identified to enhance the Chip-RET program's impact. Adding more structure, such as clear goals, regular mentor meetings, and scaffolding for challenging content, could better support participants. Bridging the program content to classroom application remains a challenge; one-on-one planning sessions and ongoing academic-year support may help.

Table 1: Summary of Results

	Pre-test	**Post-test**		
Construct	Mdn./Std. error	Mdn./Std. error	W	p
Content Test (% correct): Pre to Post	40.00 (3.29)	66.67 (3.81)	3	0.001
Content Test (% correct): Pre to Post (9 mo.)	40.00 (3.29)	53.33 (3.41)	12	0.007

Feedback suggests tailoring the pSEMI and ZeroToASIC speaker series to participants' backgrounds, making sessions more interactive. Additionally, incorporating informal facilitator meetings and social gatherings to build community is recommended. Accessibility improvements, such as ensuring accommodations like closed captioning, should be addressed proactively. In Year Two, formative feedback showed challenges in week three, resolved by week four, suggesting a review of week three content could inform future improvements. Additional support for final presentations would also help participants succeed. Implementing these changes can enhance program effectiveness and long-term impact. Finally, follow-up refresher sessions are currently being considered for past RET participants so that they can regain some of the knowledge lost after leaving the RET program.

Conclusion

The Chip-RET program has successfully equipped K-14 STEM educators with essential semiconductor knowledge, enabling them to inspire the next generation of microelectronics professionals. Teachers in both program years demonstrated significant improvements in their understanding, with Year One participants retaining much of their knowledge nine months post-training, underscoring the program's effectiveness and long-lasting impacts.

Acknowledgment

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