

Integrating Full-Featured and Freely-Downloadable Circuit Simulation Software into Multiple EET Courses

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Abstract

This paper presents the integration of *LTspice*, a full-featured and freely-downloadable circuit simulation software, into multiple Electronics Engineering Technology (EET) courses, including electric circuits, analog and digital electronics, power electronics, signals and systems, control systems, and communication systems. Integrating a free and powerful circuit simulation software in multiple courses enhances both face-to-face and online/remote modes of instruction. Additionally, three of the five Criterion-3 student outcomes specified by ABET-ETAC can be easily addressed and assessed within the simulation environment. Numerous example simulations are included encompassing various disciplinary areas to support multiple courses in a typical EET curriculum.

Introduction

This paper presents the integration of *LTspice*, a full-featured and freely-downloadable circuit simulation software, into multiple EET courses, including electric circuits, analog and digital electronics, power electronics, signals and systems, control systems, and communication systems. The software uses a powerful SPICE engine, in addition to schematic capture and waveform viewing capabilities. Its behavioral voltage and current sources in combination with dependent sources make the integration of mathematical and system-level work, in addition to traditional circuit-level simulation work, highly attractive for EET and related curriculums. Additionally, applications of mathematics (differentiation and integration, differential equations, and Laplace and Fourier transforms) for analysis, modeling, design, and simulation of engineering systems can be easily implemented within the LTspice environment. System-level design concepts such as user-defined components and devices, subcircuits, hierarchical circuits, and worst-case performance analysis are supported by LTspice as well.

Integrating a free and powerful circuit simulation software in multiple courses enhances both face-to-face and online/remote modes of instruction. Additionally, the three of the five Criterion-3 student outcomes specified by ABET-ETAC can be easily addressed and assessed within the simulation environment. The program criteria specific topics for EET type programs, such as application of mathematics to characterize the performance of electrical/electronic systems, can be easily incorporated into and assessed within the same simulation environment. Why choose LTspice over other commonly used SPICE based circuit simulation software such as PSpice and NI Multisim? The main reason is that LTspice is both full-featured and freely downloadable [1], [2]. A major advantage of using LTspice is that it is free to students and faculty in the truest sense; i.e., no licensing expiration issues, and no limitations in terms of number of components and/or circuit nodes. There is also no limit to the types of simulation that can be run (dc operating point, transient, ac analysis, dc sweep, small signal transfer function, and noise analysis). Numerous SPICE directives are available, including parametric analysis, temperature analysis, Fourier analysis, and Monte Carlo analysis. The simulation skillset developed using LTspice will transfer easily to other Spice-based packages such as PSpice and NI Multisim.

It is to be noted that circuit simulation is an important pedagogical tool that can be used to augment the process of theoretical analysis, design, and laboratory experimentation. Specifically, the theoretical analysis based designs can be verified as well as improved upon using a simulation tool, before the circuit prototyping and laboratory testing phase begins.

Numerous examples of circuits and systems design, modeling, and simulation using LTspice are presented in this paper. Specific examples cover various disciplinary areas within EET type curriculums such as circuit analysis, analog and digital electronics, power electronics, signals and systems, differential equations, Laplace and Fourier transforms, control systems, and communication systems.

Supporting Criterion-3 Student Outcomes and Program Criteria Topics

A circuit simulation software such as LTspice can be effectively used as an instructional tool to meet specific objectives of multiple EET courses. Collectively, the analysis based design and simulation experience supports three of the five ABET-ETAC *Criterion-3* student outcomes as shown in Table I. Additionally, as shown in Table II, the analysis based design and simulation experience also supports four of the five *Program Criteria* topics for Electrical/Electronics Engineering Technology programs.

Table I: Supported ABET-ETAC *Criterion-3* Student Outcomes [3]

1	an ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly-defined engineering problems appropriate to the discipline
2	an ability to design systems, components, or processes meeting specified needs for broadly-defined engineering problems appropriate to the discipline
4	an ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results to improve processes

Table II: Supported ABET-ETAC *Program Criteria* Topics for Electrical/Electronics Engineering Technology Programs [3]

The curriculum must include the following topics:	
a	application of circuit analysis and design, computer programming, associated software, analog and digital electronics, microcontrollers, and engineering standards to the building, testing, operation, and maintenance of electrical/electronic(s) systems
b	application of natural sciences and mathematics at or above the level of trigonometry to the building, testing, operation, and maintenance of electrical/electronic systems
c	analysis, design, and implementation of one or more of the following: control systems, instrumentation systems, communications systems, computer systems, power systems or energy systems
e	utilization of differential and integral calculus, as a minimum, to characterize the performance of electrical/electronic systems

Students can be assessed for specific performance indices linked to the course objectives, Criterion-3 student outcomes, and program criteria topics. Additionally, performance index-based direct assessment of student outcomes provides valuable input to the program-level continuous improvement process.

LTspice Simulation Examples Applicable to Multiple EET Courses

R-C charging/discharging circuit simulation

A capacitor charging and discharging circuit simulation is shown in Fig. 1. The simulation circuit uses two switches controlled by the two piecewise linear voltage sources. The simulated waveforms clearly show that the charging is completed in about 30 ms while the discharging is completed in about 40 ms, verifying the five time constants rule of thumb for complete charging and discharging. The peak charging and discharging currents of 8 mA and -6mA, respectively, can also be verified using the Ohm's law.

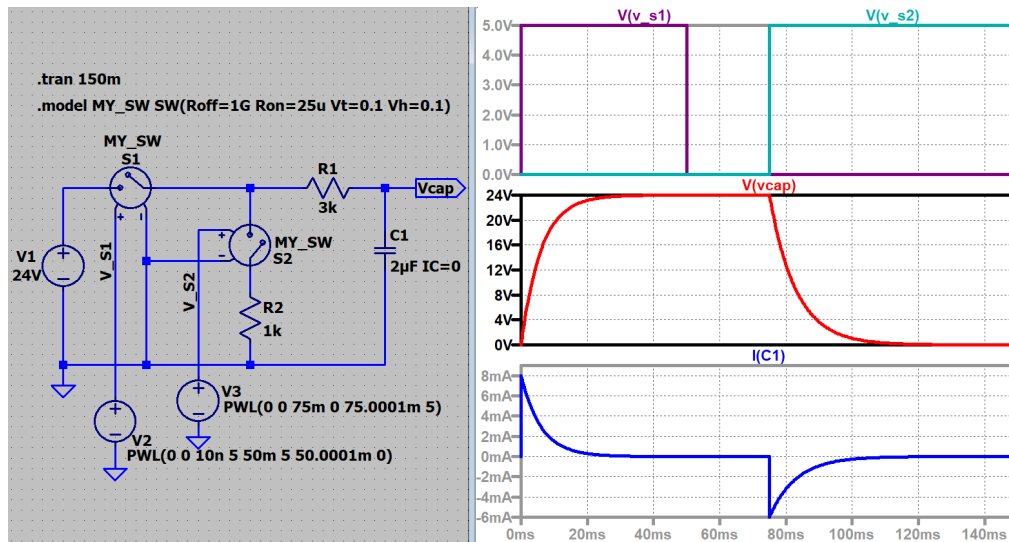


Figure 1: Capacitor charging and discharging simulation

AC circuit simulation: Phasor domain

Simulation of an ac circuit in phasor domain [4] is shown in Fig. 2. The circuit consists of two ac voltage sources of the same frequency but of different amplitude and phase angle. A node-voltage method of analysis using a single node equation can be used to analyze this circuit. A quick simulation can be done in phasor domain at the frequency of interest, providing a list of all node voltages and component currents.

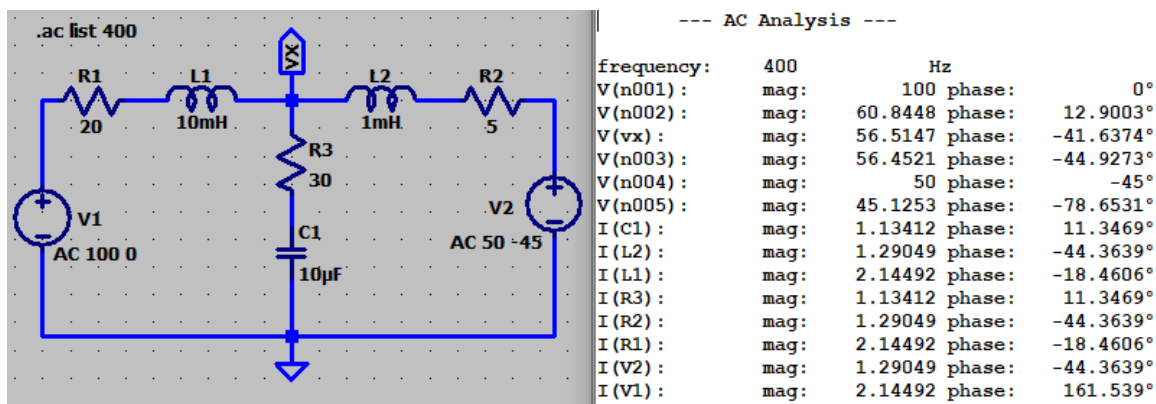


Figure 2: Phasor domain ac circuit simulation

AC circuit simulation: Maximum average power transfer condition

The resistive load for the ac circuit shown in Fig. 3 varies between 10 and 30 Ω . This circuit is excited by one voltage source and one current source of the same frequency, and the objective of the simulation is to find the maximum average power in the load and the corresponding load resistance value. By analysis a Thevenin equivalent circuit can be found consisting of a Thevenin voltage of $29.81\angle -92.81^\circ$ V and a Thevenin impedance of $17.92\angle -9.56^\circ \Omega$. Using the maximum average power transfer condition, the maximum average load power can be calculated to be 12.49 W at a load resistance value of 17.92 Ω . The simulation verifies the maximum power transfer condition, within the expected cursor setting error. It is to be noted that for simulation purpose a frequency of $1/(2\pi)$ Hz is used in order to be able to use the inductive and capacitive reactance values from the original circuit.

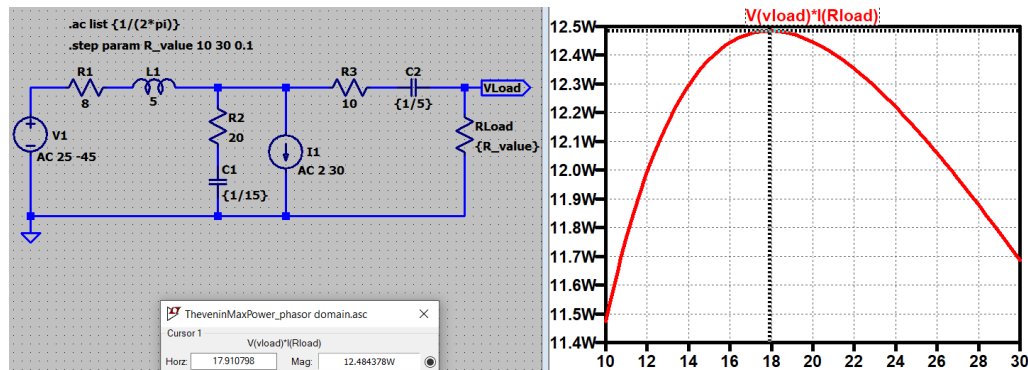


Figure 3: Simulation for maximum average power in an ac circuit

AC circuit simulation: Real/Reactive/Apparent power and Power Factor calculations

For the circuit shown in Fig. 4, the real and reactive power for each of the three parallel loads can be calculated using the power triangle concept, leading to the establishment of a power triangle for the combined or total load [4] on the 240 VAC line. An analysis for the total load system results the following: real power of 8837.5 W, reactive power of 3218.9 VAR, apparent power of 9405.5 VA, a power factor of 0.94 (lagging), and a supply rms current of 39.2 A.

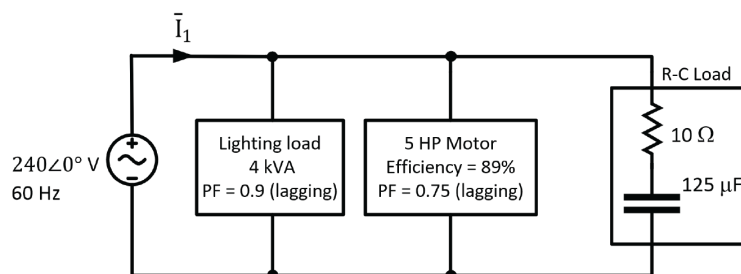


Figure 4: An example ac circuit with multiple loads in parallel

This load system was simulated in LTspice, as shown in Fig. 5. Each of the three loads was represented as a series circuit, and the variables of interest for the load system were calculated using the *.meas* function within LTspice. The simulation results are: real power of 8837.68 W, reactive power of 3218.58 VAR, apparent power of 9405.52 VA, a power factor of 0.94

(lagging), and a supply rms current of 39.2 A. All of these values are practically the same as the ones obtained by analysis.

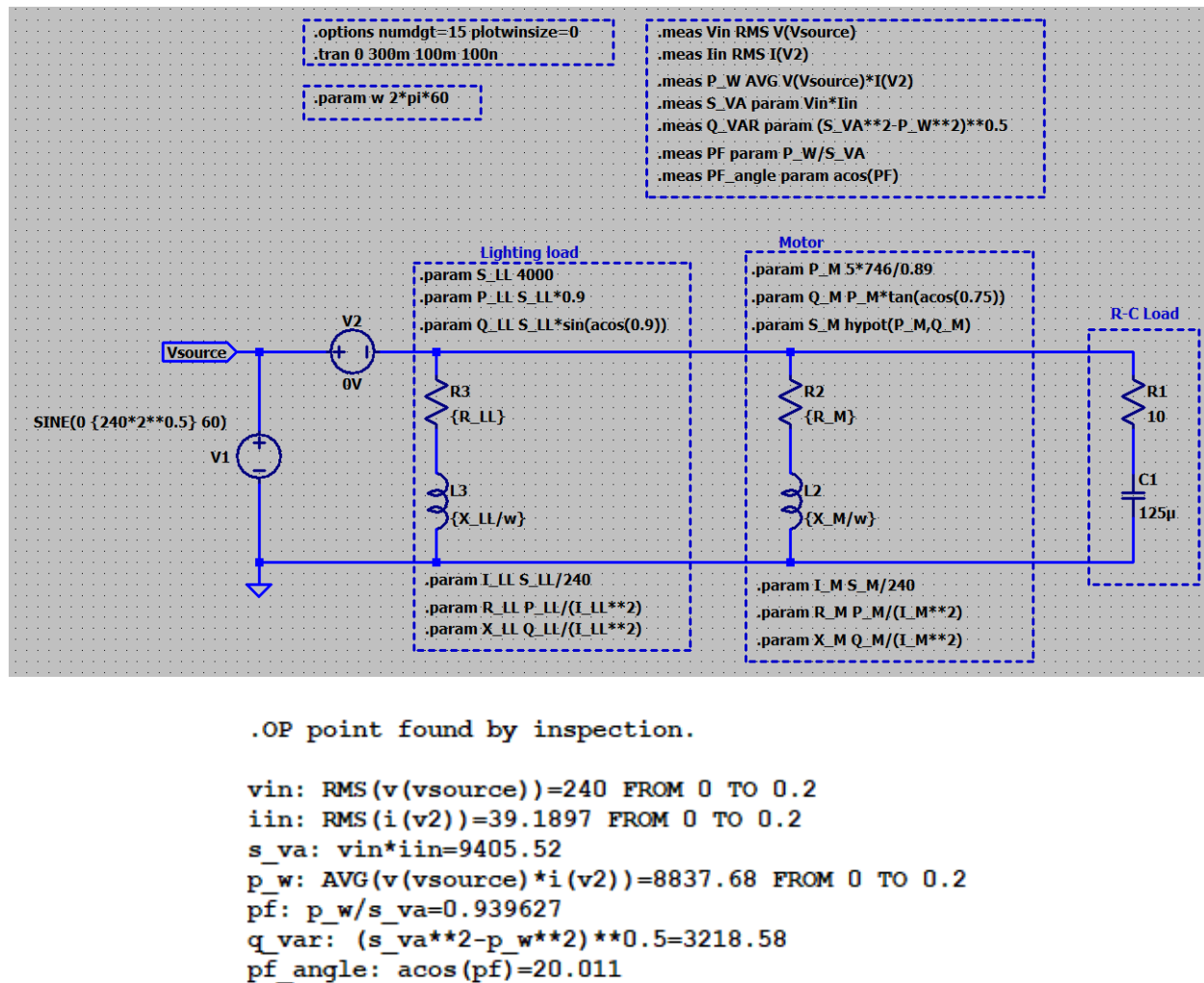


Figure 5: AC power simulation (top) and the output results for the variables of interest (bottom)

AC circuit simulation: Center-tapped power distribution transformer

A typical center-tapped power distribution transformer circuit supplying power to 120 VAC loads ($12\ \Omega$ connected between L1-N and $10\ \Omega$ connected between L2-N) and 240 VAC loads ($12\ \Omega$ connected between L1-L2) is shown in Fig. 6. The distribution transformer steps down the incoming 12 kV to a typical 120 V/240 V residential utility power source. Since inductance is proportional to square of the number of its turns, a turns ratio of 100 is achieved in the simulation schematic using inductances of 10 H (primary) and 1 mH (secondaries). The simulated waveforms clearly show the expected relationships among the various load voltages and currents, including the non-zero neutral current due to the load imbalance between line 1 and line 2.

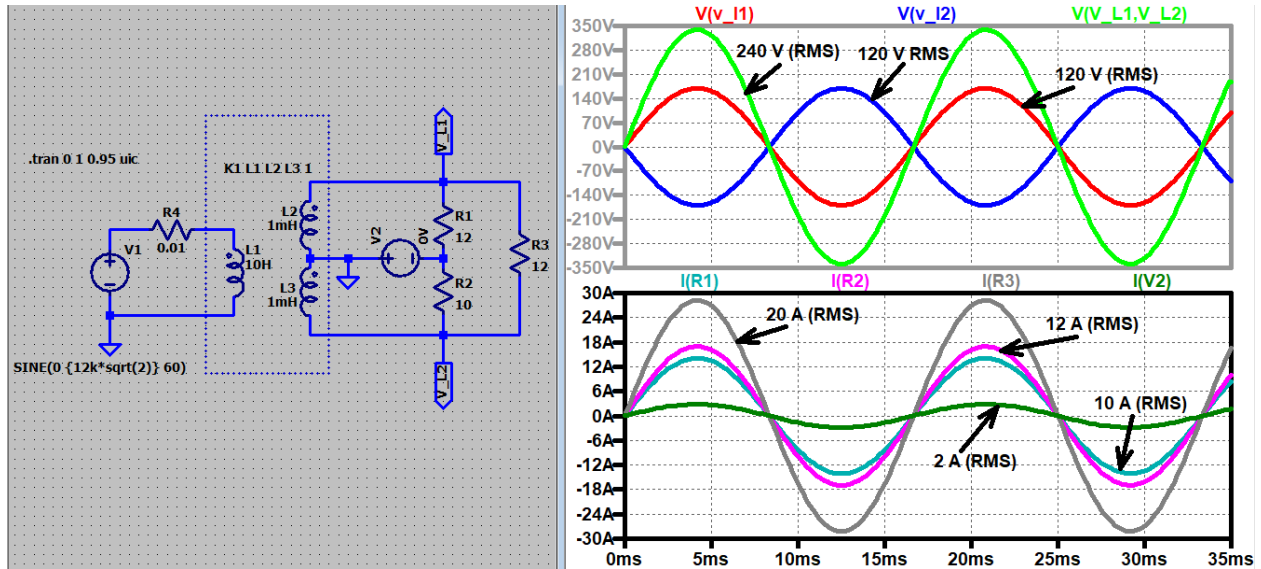


Figure 6: simulation of an ideal center-tapped power distribution transformer

Three-phase diode rectifier circuit simulation

A three-phase diode rectification simulation circuit with a capacitive filter is shown in Fig. 7. The theoretical peak value of the rectified output voltage is $293.94 \text{ V} (= 120 \times \sqrt{2} \times \sqrt{3} \text{ V})$ whereas the measured average value of the output voltage is 287.24 V . This represents a peak output ripple of 6.7 V , i.e., the output ripple voltage is 2.33% of the average output voltage. A peak-to-peak ripple of 4.66% would be acceptable in some applications, however, for applications with a tighter ripple requirement will require additional filtering. The capacitor current waveform clearly shows there are six charging/discharging cycles within one cycle of input ac voltage, thus the frequency of the rectified output voltage is 360 Hz for a 60 Hz ac input. It is to be noted that the fundamental concept of average current in a capacitor shall be zero for cyclic operation can be visually verified from the capacitor current waveform.

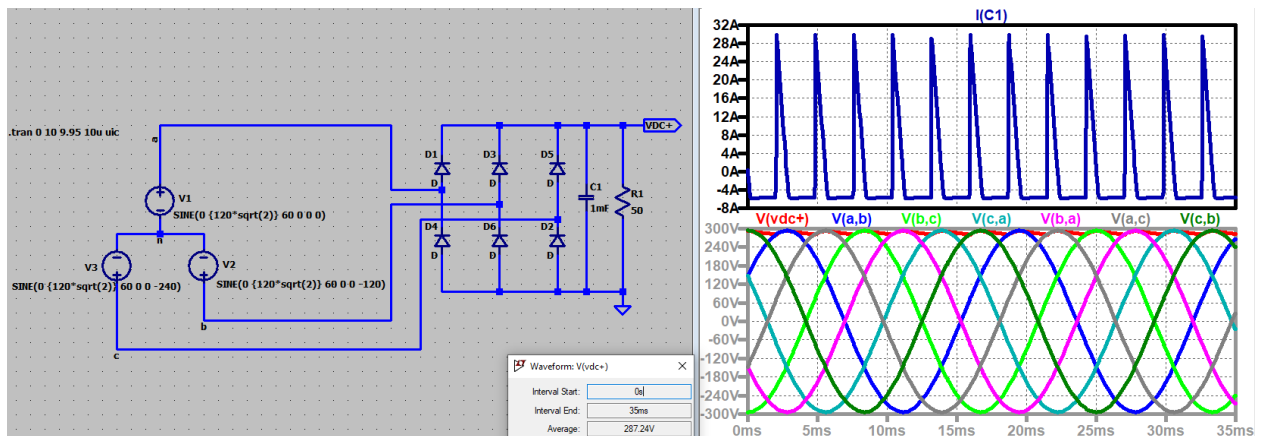


Figure 7: Simulation of a three-phase diode rectifier circuit

Two-stage broadband amplifier with feedback

This example presents the simulation of a broadband amplifier [5] for a $75\ \Omega$ communication system with the following specifications: input and output resistances are both $75\ \Omega$, a minimum gain of 6 dB, use only a 12 VDC source, and the gain must be constant in the 1 kHz to 10 MHz range. The simulation circuit for the amplifier as shown in Fig. 8 uses a 100 mV (peak), 1 kHz sinusoidal input. The peak of the output is about 218 mV, i.e., the amplifier's gain is about 6.77 dB and thus meets the amplification requirement. The two common emitter stages produce a total phase shift of 360° , resulting in output and input voltages in phase.

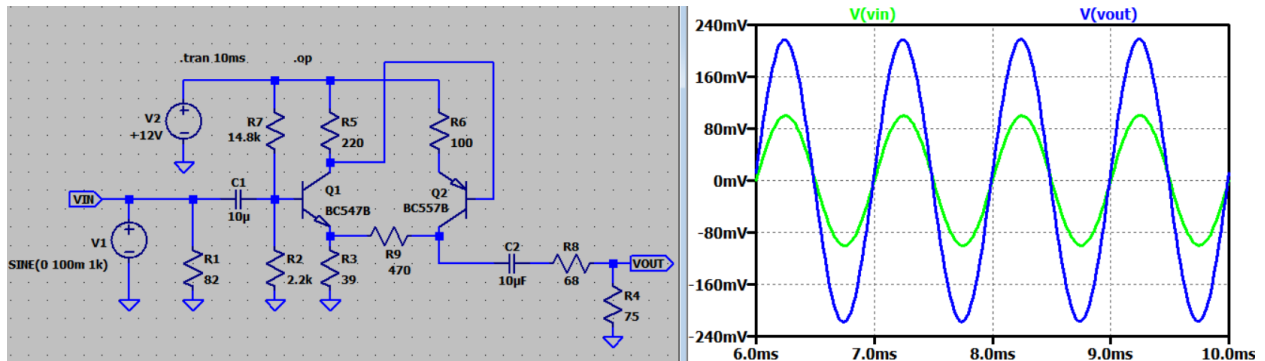


Figure 8: Simulation of a broadband amplifier circuit

Performing an *ac analysis* of the amplifier circuit in the 1 Hz to 200 MHz range provides the frequency response as shown in Fig. 9. The gain is about 6.78 dB and it is practically constant in the range of interest (1 kHz to 10 MHz), satisfying the bandwidth requirement. A phase shift of practically zero degrees is achieved in the range of 1 kHz and 3 MHz, implying that design of the amplifier needs to be further optimized in the 3 to 10 MHz range.

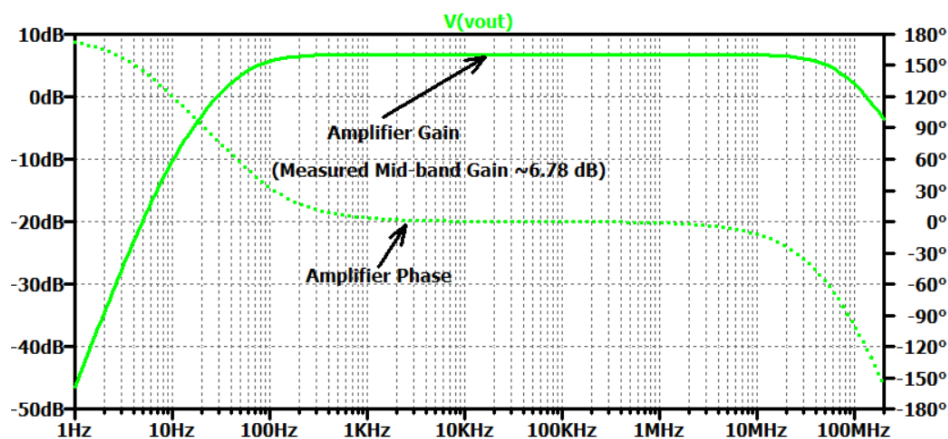


Figure 9: Frequency response of the simulated broadband amplifier circuit

Frequency response simulation of an active filter circuit

The bandpass filter shown in Fig. 10 was designed to achieve a gain of 20 dB over the 20 Hz to 20 kHz range, using the standard value passive components. The derived transfer function of the circuit is expressed in (1).

$$\frac{V_{out}(S)}{V_{in}(S)} = -\frac{(1.22 \times 10^6)S}{\{S + 2\pi(19.4)\}\{S + 2\pi(19.4 \times 10^3)\}} \quad (1)$$

The simulated frequency response does show a zero at the origin, a pole at about 20 Hz, and a second pole at about 20 kHz. The gain crossover frequencies are approximately at 2 Hz and 200 kHz, justifying the mid-band gain of 20 dB. As expected, the phase angle is -90° at low frequencies, -180° at mid-band frequencies, and -270° at higher frequencies.

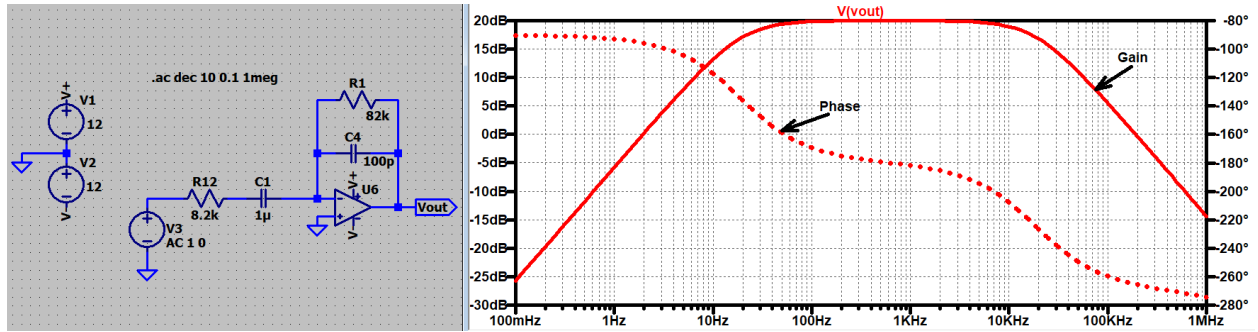


Figure 10: Frequency response of the simulated active bandpass filter circuit

555 Timer circuit simulation

The astable operation of a 555 timer circuit is shown in Fig. 11. As expected, the capacitor is charging and discharging between the threshold voltage (8 V) and trigger voltage (4 V) levels. For the selected component values, the theoretical charging time, discharging time, and output frequency are 589.05 μ s, 395.01 μ s, and 1.016 kHz. The simulated waveforms match with the expected waveforms, including the measured switching frequency of 1.016 kHz.

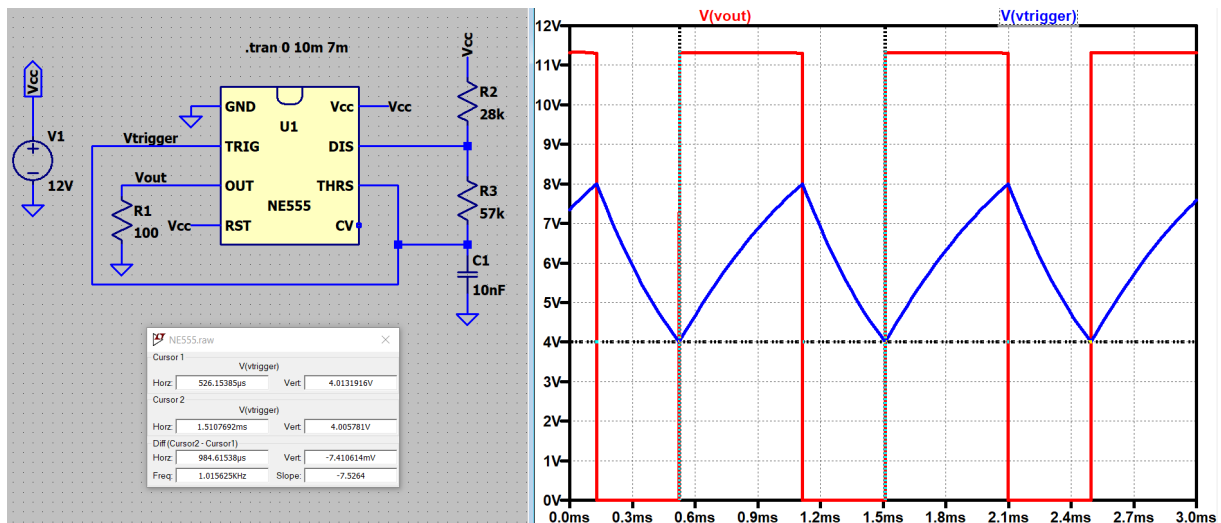


Figure 11: Trigger and output voltages of the simulated 555 timer circuit

SCR-based rectifier circuit simulation

An SCR-based full-wave controlled rectifier circuit with a firing angle of 45° was simulated as shown in Fig. 12. The simulated output voltage waveform is as expected, and the effect of SCR's forward voltage drop is clearly visible at the peak current of approximately 8 A (= 160 V/20 Ω). Using an SCR with a lower on resistance would have resulted in a lower voltage drop, thus resulting in an increased average output voltage.

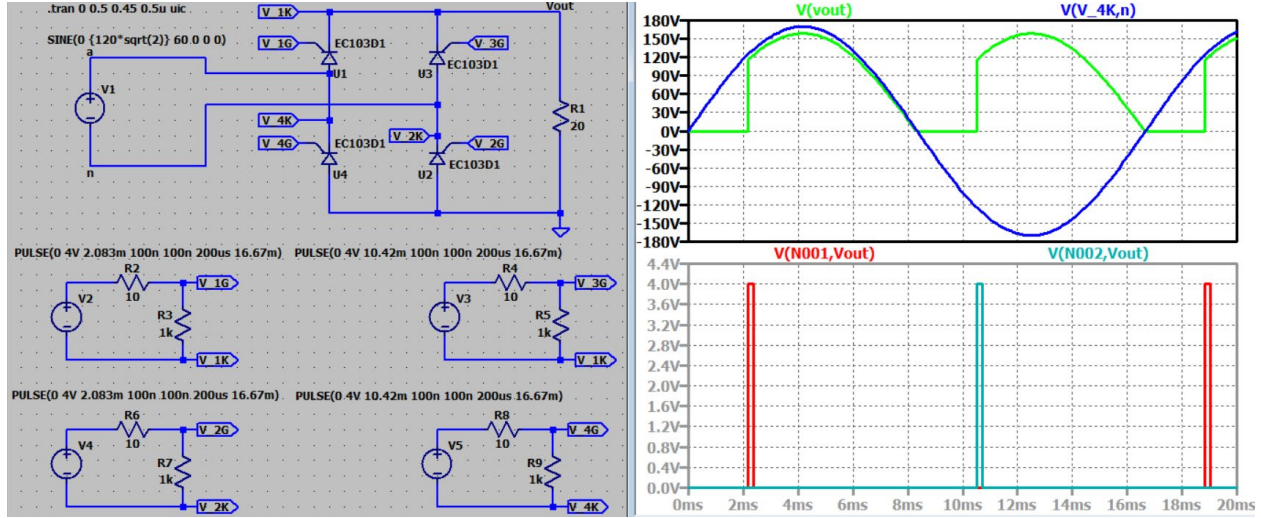


Figure 12: Simulation of a full-wave controlled rectifier circuit

Single-phase PWM DC-AC inverter circuit simulation

A single-phase full-bridge inverter circuit was simulated with unipolar pulse width modulation (PWM), as shown in Fig. 13. In a unipolar PWM switching [6], a high frequency triangular carrier ($v_{tri,carrier}$) is compared with two low frequency sinusoidal references ($v_{sine,ref}$). Consequently, device M1 is on when $v_{sine,ref} > v_{tri,carrier}$, device M2 is on when $-v_{sine,ref} < v_{tri,carrier}$, device M3 is on when $-v_{sine,ref} > v_{tri,carrier}$, and device M4 is on when $v_{sine,ref} < v_{tri,carrier}$. The example schematic uses the concepts of amplitude modulation ratio ($m = V_{sine,ref}/V_{tri,carrier}$) and frequency modulation ratio ($m_f = f_{tri,carrier}/f_{sine,ref}$). The circuit of Fig. 13 was simulated with an amplitude modulation ratio (m) of 0.7, a sinusoidal reference frequency ($f_{sine,ref}$) of 50 Hz, and a carrier frequency ($f_{tri,carrier}$) of 1150 Hz. This represents a frequency modulation ratio (m_f) of 23.

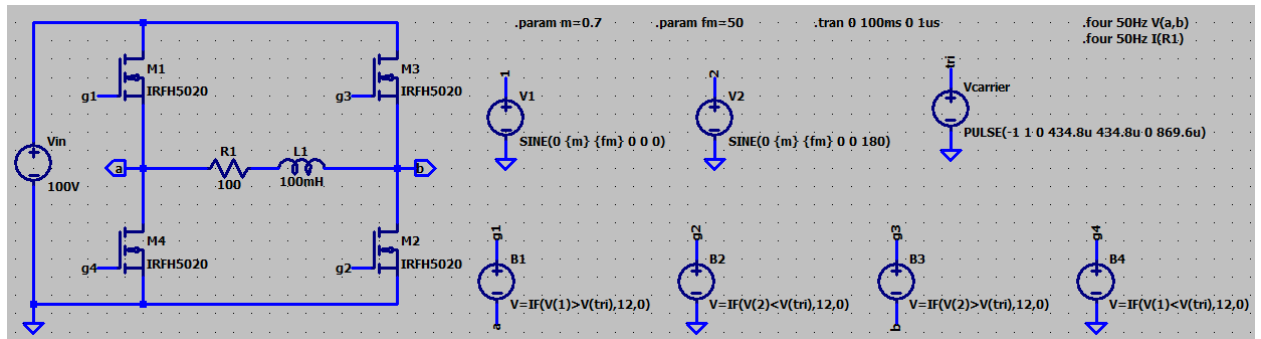


Figure 13: Simulation schematic of a single-phase PWM dc-ac inverter circuit

One cycle of the simulated load current and load voltage waveforms is shown in Fig. 14, and the PWM switching can be clearly observed in the load voltage waveform. The load current looks closer to a sinusoid; however, as expected it includes higher frequency components. The higher frequency components are of much lower amplitude compared to the 50 Hz fundamental component since the load inductance acts as an effective filter at higher frequencies.

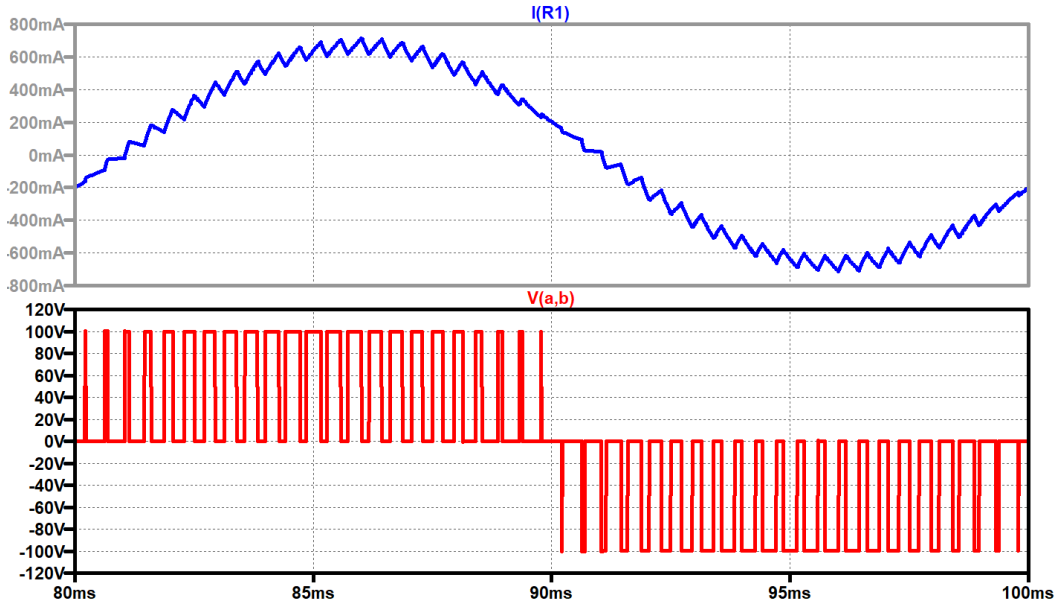


Figure 14: Simulated load current and load voltage of the single-phase PWM inverter

The output voltage, however, doesn't intuitively look like a sinusoid. This is where a Fourier analysis is needed; the LTspice generated Fourier components of the load voltage are shown in Fig. 15. It can be observed that the peak value of the fundamental component at 50 Hz is practically 70 V, it is consistent with the expected value (multiplication of the amplitude modulation ratio of 0.7 with the input dc voltage of 100 V). The table in Fig. 15 lists the first nine harmonic components; the third and fifth harmonics at 150 Hz and 250 Hz, respectively, contribute the most but only by about 0.02%. This confirms the effectiveness of PWM modulation technique in power conversion circuits.

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component
1	5.000e+1	6.998e+1	1.000e+0
2	1.000e+2	3.750e-3	5.359e-5
3	1.500e+2	1.404e-2	2.007e-4
4	2.000e+2	1.486e-3	2.123e-5
5	2.500e+2	1.453e-2	2.076e-4
6	3.000e+2	9.473e-3	1.354e-4
7	3.500e+2	1.111e-2	1.588e-4
8	4.000e+2	1.069e-2	1.527e-4
9	4.500e+2	1.043e-2	1.490e-4

Figure 15: Fourier components of the inverter load voltage

Digital circuit simulation: Frequency divider with D flipflops

The simulation schematic of a frequency divider circuit with three D flipflops is shown in Fig. 16. With three flipflops the input clock frequency can be divided by 2, 4, and 8. The waveforms shown in Fig. 16 includes the 1 kHz clock as well as the output of the three flipflops at 500 Hz, 250 Hz, and 125 Hz, respectively. It is to be noted that the built-in LTspice library is light in the availability of standard TTL and CMOS digital parts, however, the LTspice user group webpages [7], [8] can be accessed for many commonly used digital parts.

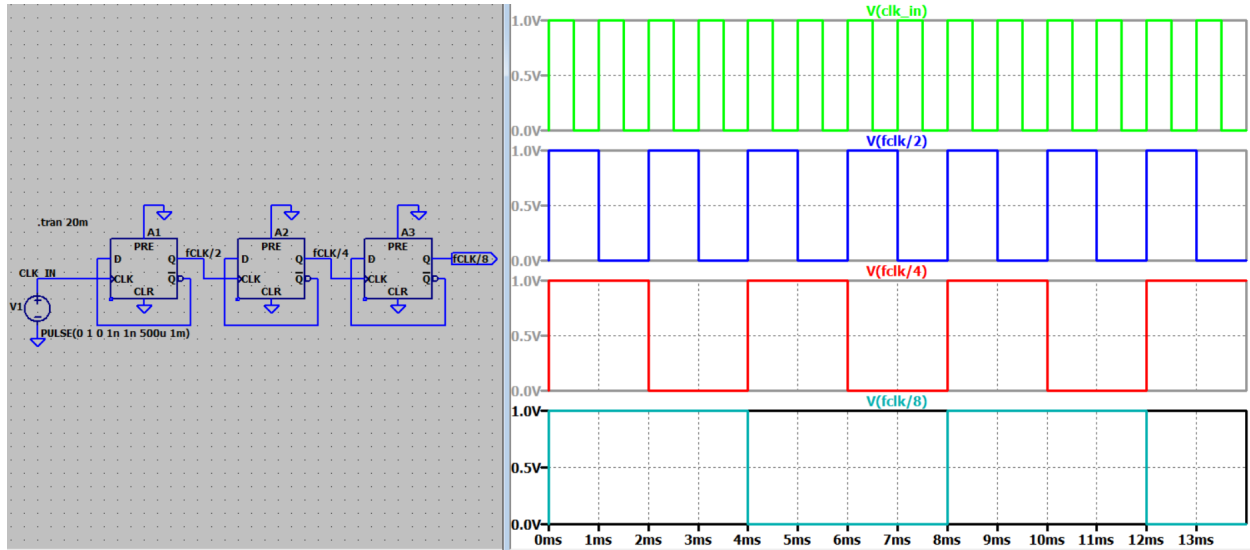


Figure 16: Simulation of a frequency divider circuit with D flipflops

Simulating differential equations

Consider a typical second-order differential equation along with the initial conditions given in (2). This type of equation is a common occurrence in analyzing linear systems.

$$\frac{d^2v}{dt^2} + 3\frac{dv}{dt} + 2v = 10 \sin(2t); \quad v(0) = 1, \quad \frac{dv}{dt}(0) = -1 \quad (2)$$

The analytical solution of (2) can be obtained using the concepts of complementary function (transient) and particular integral (steady state). The complete solution to (2) is given in (3).

$$v(t) = 5e^{-t} - 2.5e^{-2t} - 1.5 \cos(2t) - 0.5 \sin(2t) \quad (3)$$

The above solution can be presented in a more compact form as in (4).

$$v(t) = 5e^{-t} - 2.5e^{-2t} + 1.581 \sin(2t - 108.43^\circ) \quad (4)$$

The time domain plot of $v(t)$ can be obtained in LTspice as shown in Fig. 17. The initial value of 1 V, steady state amplitude of 1.581 V, and a steady state oscillation frequency of 2 rad/s (corresponding to a time period of 3.142 s) can be visually verified in the plot of Fig. 17. It can also be observed that the transients are dying out in approximately 5 s, consistent with the five time constant rule since the largest time constant in (4) is 1 s.

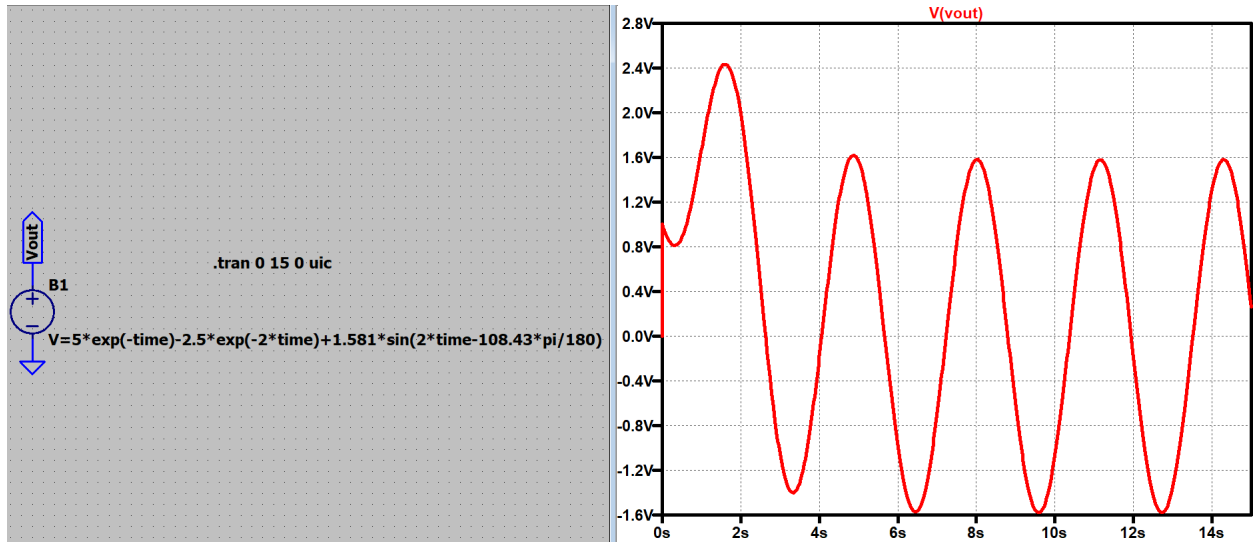


Figure 17: Voltage waveform simulation using the time domain expression of the differential equation solution

The time domain plot of $v(t)$ can also be obtained by simulating the differential equation using op-amps [9]. The LTspice circuit implementation using three op-amps (one integrator, one summing integrator, and one inverter) is shown in Fig. 18. The output voltage waveform in Fig. 18 matches with the analytical one in Fig. 17. Using the cursor measurement, the steady state phase lag of the output in time is 945.4 ms, corresponding to a phase lag of 108.3° ($= 945.4 \text{ ms} \times 360^\circ / 3.142 \text{ s}$), practically identical to the analytical phase shift of 108.43° .

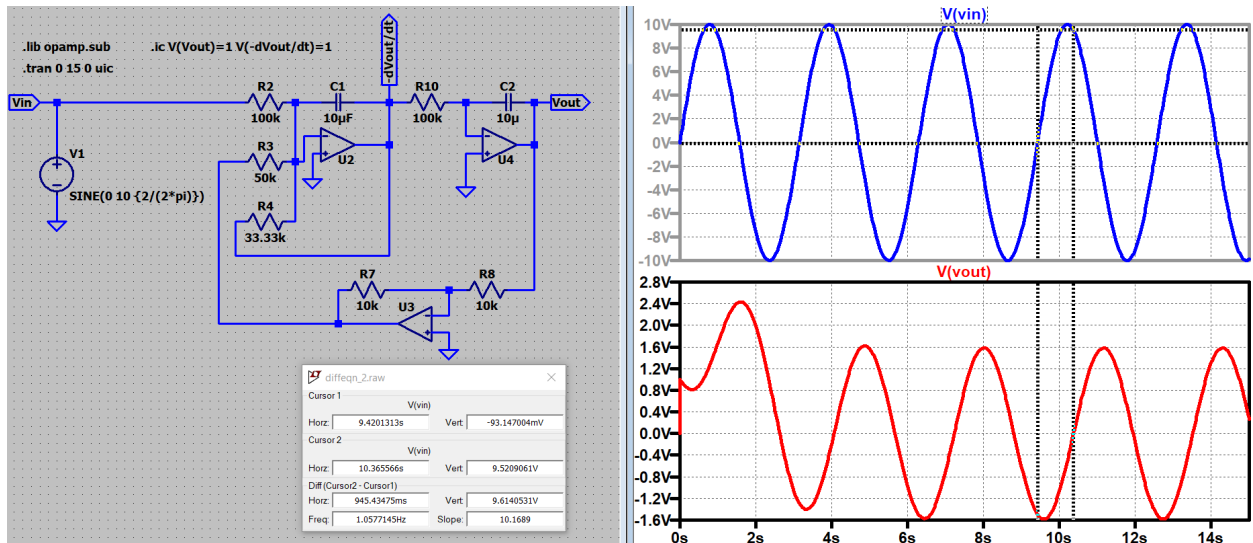


Figure 18: Simulation of the differential equation using op-amps

The differential equation of (2) can also be solved using Laplace transform. Applying Laplace transform to (2) with the given initial conditions, results in (5).

$$V(S) = \frac{20}{(S^2 + 4)(S^2 + 3S + 2)} + \frac{1}{S + 1} \quad (5)$$

The Laplace function in LTspice [10] is used to obtain the $v(t)$ waveform, as shown in Fig. 19. Again, this plot matches with the previous two plots for $v(t)$. The use of Laplace function within LTspice opens the door to designing control systems as discussed next.

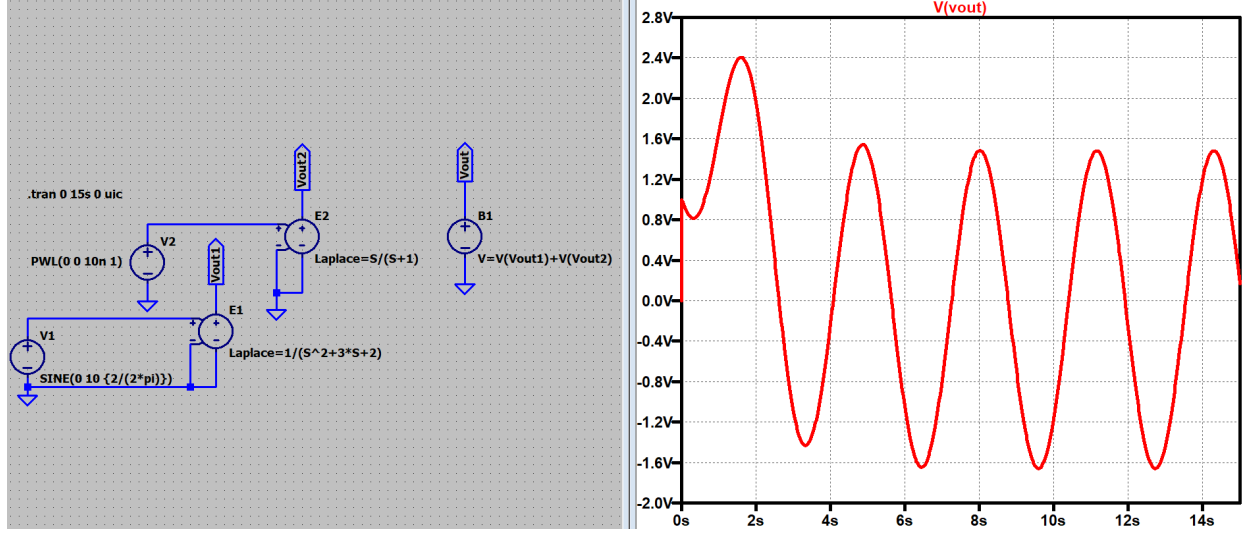


Figure 19: Simulation of the differential equation using Laplace transform expressions

Feedback control system simulation: DC-DC switching power converter

The power stage of a dc-dc switching converter was designed per the following specifications: input voltage of 10 V, output voltage of 5 V, output power of 10 W, switching frequency of 100 kHz, output capacitor ESR of 0.25 Ω , and a peak-to-peak inductor ripple current limited to 12.5% of the load current. The resulting power stage and the simulated output voltage waveform are shown in Fig. 20 for full load operation with a duty ratio of 0.5. The cursor measurement shows a peak-to-peak output voltage ripple of 56.49 mV; thus it is about 1.13% of the output voltage, an acceptable value for many applications.

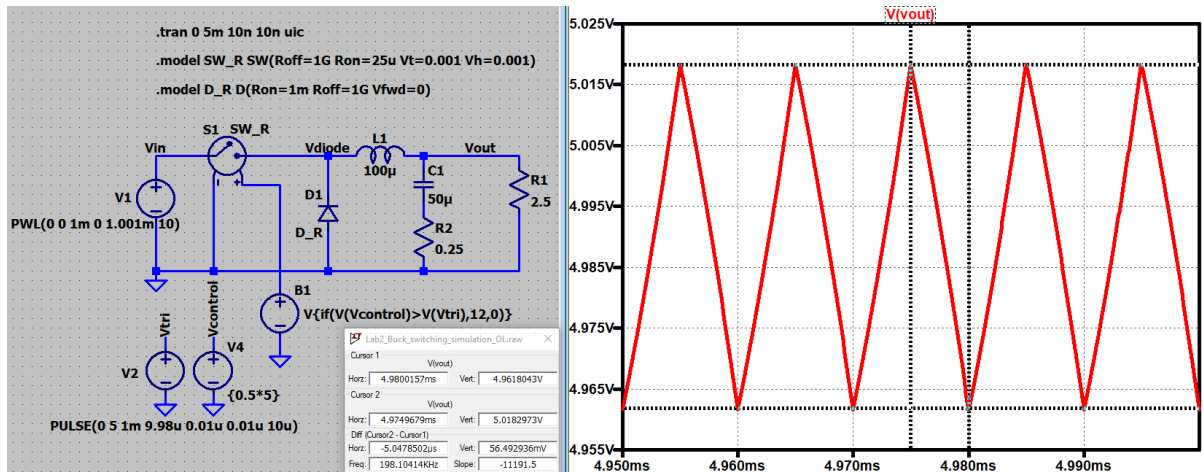


Figure 20: Simulation of the power stage of a dc-dc switching power converter

Next a feedback loop is designed to regulate the output voltage against load current and input voltage variations. The closed loop design specifications to be satisfied are: a loop gain crossover frequency of 20 kHz, a phase margin of 45° for stability, and a sawtooth peak voltage of 3 V (used to generate PWM pulses). However, before a feedback controller can be designed, a transfer function of the power stage (output voltage to duty ratio) needs to be known. Accordingly, an average model [11] of the power stage was derived and the resulting expression is given in (6).

$$\frac{V_{out}(S)}{D(S)} = V_{in} \left(\frac{S + 80 \times 10^3}{80 \times 10^3} \times \frac{200 \times 10^6}{S^2 + 10.5 \times 10^3 S + 200 \times 10^6} \right) \quad (6)$$

An ac analysis of the power stage was conducted using the circuit model as well as the derived transfer function, as shown in the top section of Fig. 21. The corresponding power stage frequency responses are shown in Fig. 22 using the circuit model as well as the mathematical model. The two plots are practically identical, confirming the validity of the modeling technique. At the desired gain crossover frequency of 20 kHz, per the cursor measurement in Fig. 22, the power stage gain is -13.3 dB and phase is -118.1°. This information is essential to the design of the controller discussed next.

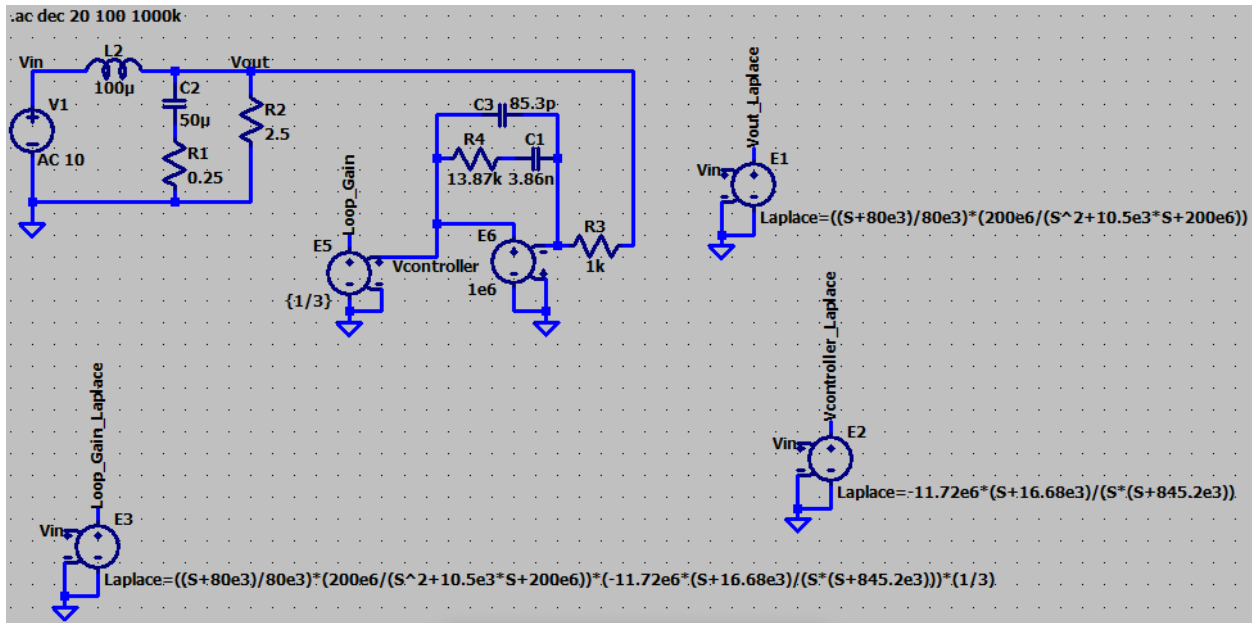


Figure 21: Simulation schematic for *ac analysis* of the dc-dc converter under open and closed loop operation (circuit model as well as mathematical model)

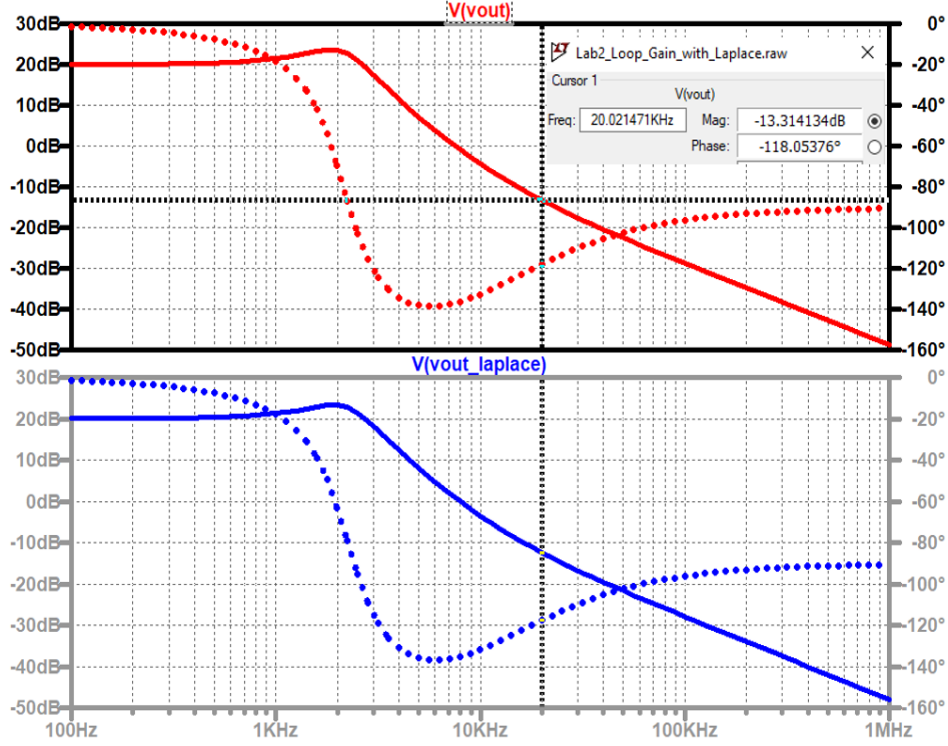


Figure 22: Frequency response of the converter power stage, circuit model response (top) and mathematical model response (bottom)

Now that the power stage frequency response is known, a type-2 controller with a pole at the origin and a pole-zero pair can be designed to meet the closed loop performance specifications stated earlier in terms of loop gain crossover frequency and phase margin. The designed controller transfer function (controller output to converter output voltage) is expressed in (7).

$$\frac{V_C(S)}{V_{out}(S)} = -\frac{11.72 \times 10^6 (S + 16.68 \times 10^3)}{S(S + 845.2 \times 10^3)} \quad (7)$$

Now the loop gain of the feedback control system can be established by multiplying the power stage transfer function of (6), controller transfer function of (7), and the PWM modulator gain of 1/3. The resulting loop gain is expressed in (8).

$$Loop_gain = \left(\frac{S + 80 \times 10^3}{80 \times 10^3} \times \frac{200 \times 10^6}{S^2 + 10.5 \times 10^3 S + 200 \times 10^6} \right) \times \left(-\frac{11.72 \times 10^6 (S + 16.68 \times 10^3)}{S(S + 845.2 \times 10^3)} \right) \times \left(\frac{1}{3} \right) \quad (8)$$

The ac analysis schematic shown in Fig. 21 includes the controller circuit configuration as well as its derived transfer function. The mathematical expression for the loop gain is also included in Fig. 21. An ac analysis of the closed loop circuit as well as the mathematical transfer functions results in the loop gain plots shown in Fig. 23. The loop gain plots using the circuit configuration as well as the derived mathematical model are practically identical. Additionally, the cursor measurement indicates that the simulated gain crossover frequency is 19.7 kHz with a phase margin of 44.9°, practically matching the closed loop design requirement.

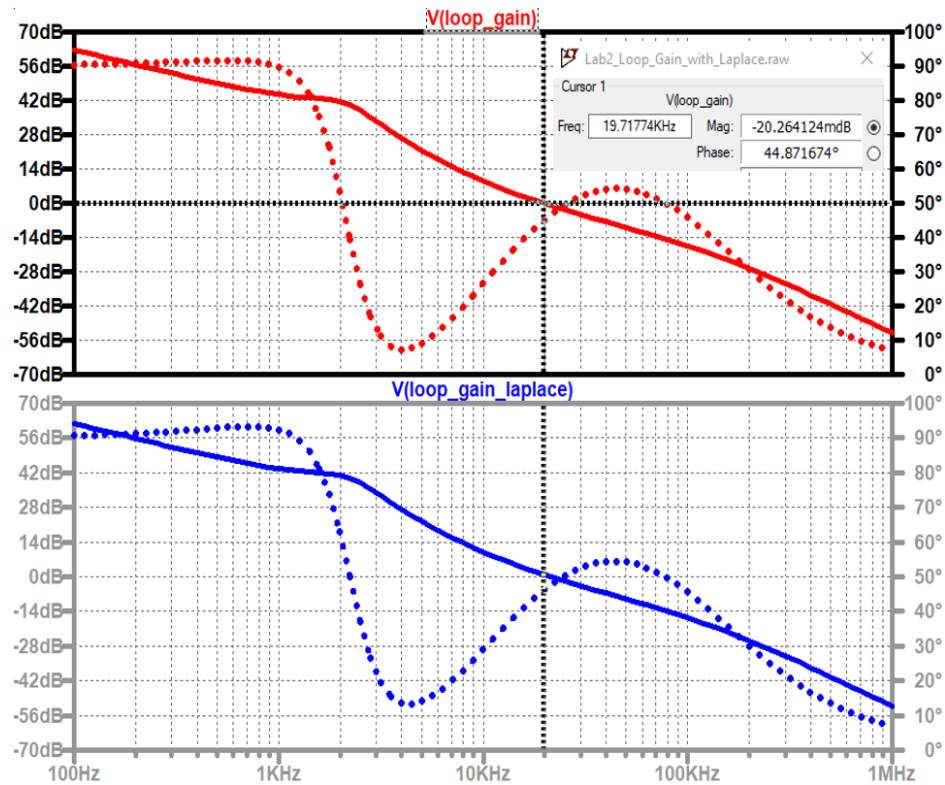


Figure 23: Control loop frequency response of the closed loop converter, circuit model response (top) and mathematical model response (bottom)

Now that the closed loop control system designed in frequency domain is in place, the switching converter's time domain performance under closed loop operation can be evaluated by applying a step change in the load current. Figure 24 shows the simulation schematic including the feedback controller, whereby the load current is switched instantly from 2 A to 4 A by changing the load resistance from 2.5 Ω to 1.25 Ω , with a reference output voltage of 5 V. The resulting simulation waveforms are shown in Fig. 25, and it can be clearly seen that as the step increase in load current takes place, the nominal output voltage of 5 V undershoots to 4.4 V followed by an overshoot to about 5.3 V, eventually reaching steady state at 5 V. Thus the output voltage transients due to a step increase in load from 2 A to 4 A is over in about 100 μ s, a reasonably fast recovery for a typical power converter. The controller output in Fig. 25 indicates how the duty ratio of the switch (S1) is adjusted during the undershoot and overshoot of the output voltage to help its transient recovery. It is to be noted that the small ripple in the output voltage during the steady state operation is an inherent characteristics of dc-dc power converters, and is determined by the open-loop power stage design.

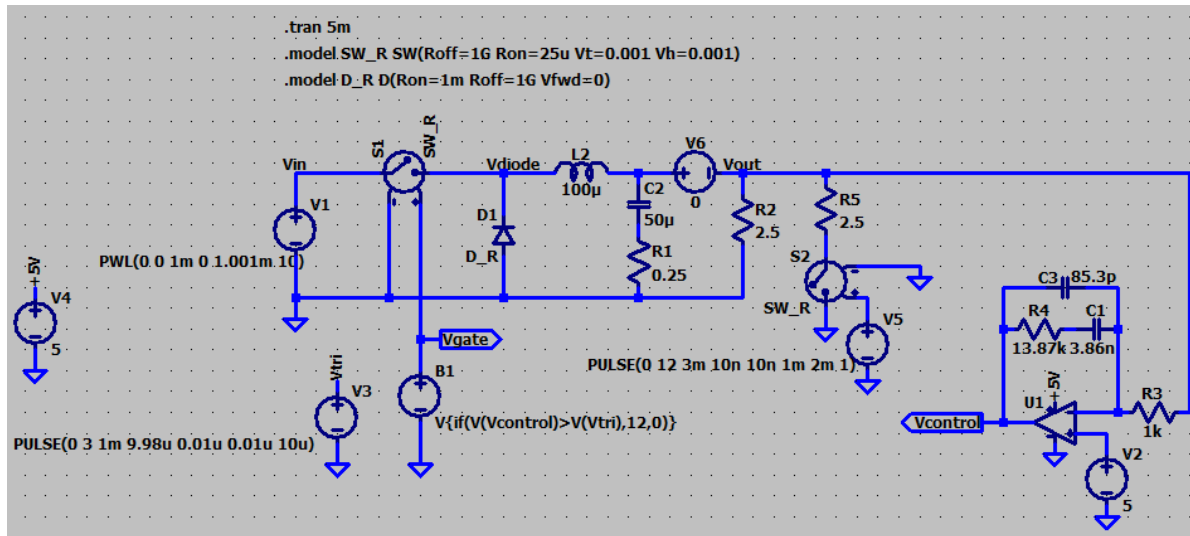


Figure 24: Simulation circuit of the closed loop converter for its time domain performance evaluation

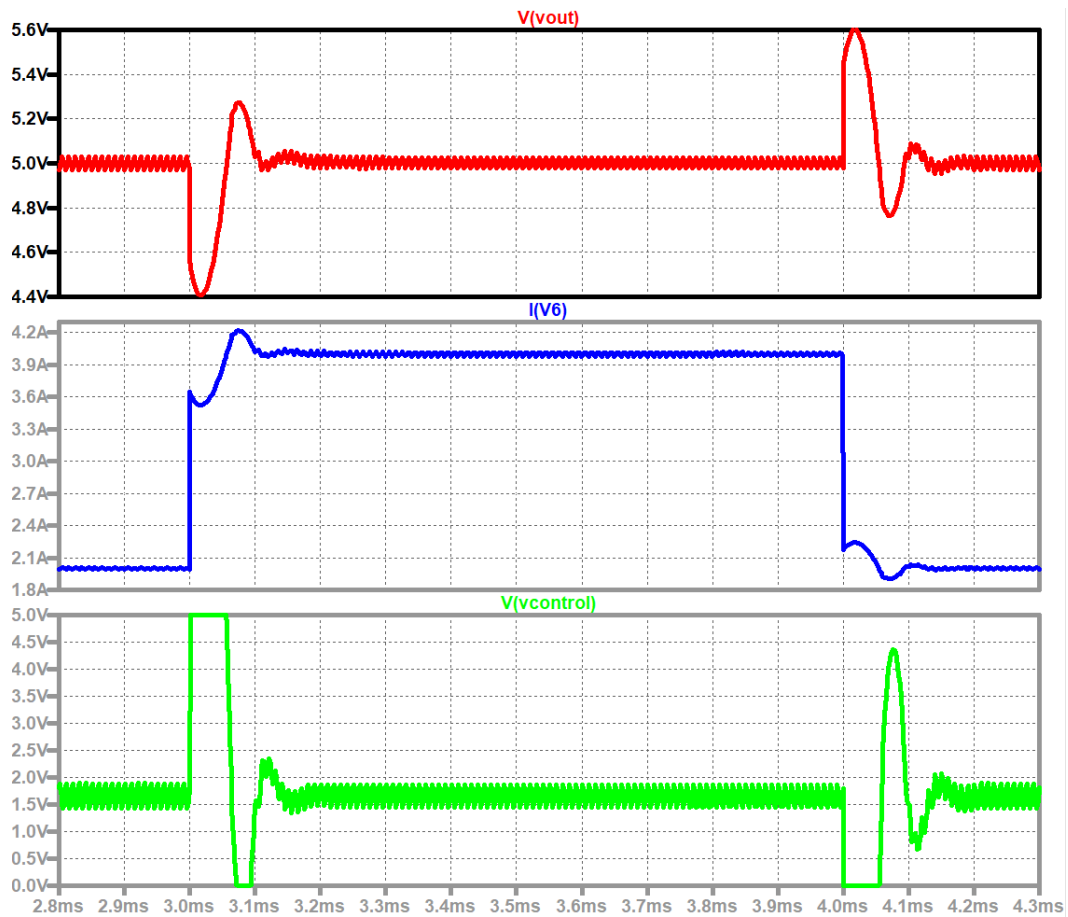


Figure 25: Key simulated waveforms illustrating the transient performance of the closed loop converter due to step load changes

Communication circuits simulation: Amplitude modulation

The basic concept of amplitude modulation (AM) is that audio signals have wavelengths that are far too large to be radiated wirelessly using antennas with an acceptable efficiency. Thus a high frequency carrier signal is used so that a smaller antenna could be used while the information is superimposed onto the carrier for transmission [12]. The amplitude of the carrier is modulated in synch with the information. Mathematically, amplitude modulation involves multiplication and addition of two different signals. A simulation of the amplitude modulation concepts [5] are shown in Fig. 26, where a 10 kHz carrier signal with a peak value of 1 V is multiplied with the 500 Hz information signal with an amplitude of 0.5 V to generate the modulation product. This modulation product is then added to the unmodulated carrier signal to generate the output AM signal. An FFT simulation of the output signal shows the carrier frequency at 10 kHz along with the lower sideband (carrier frequency minus signal frequency) at 9.5 kHz and the upper sideband (carrier frequency plus signal frequency) at 10.5 kHz. In theory, amplitude of the sidebands is half the signal amplitude, i.e., 250 mV. The FFT simulation confirms this as it shows a rms value of 176.8 mV ($= 250 \text{ mV} \times 0.707$).

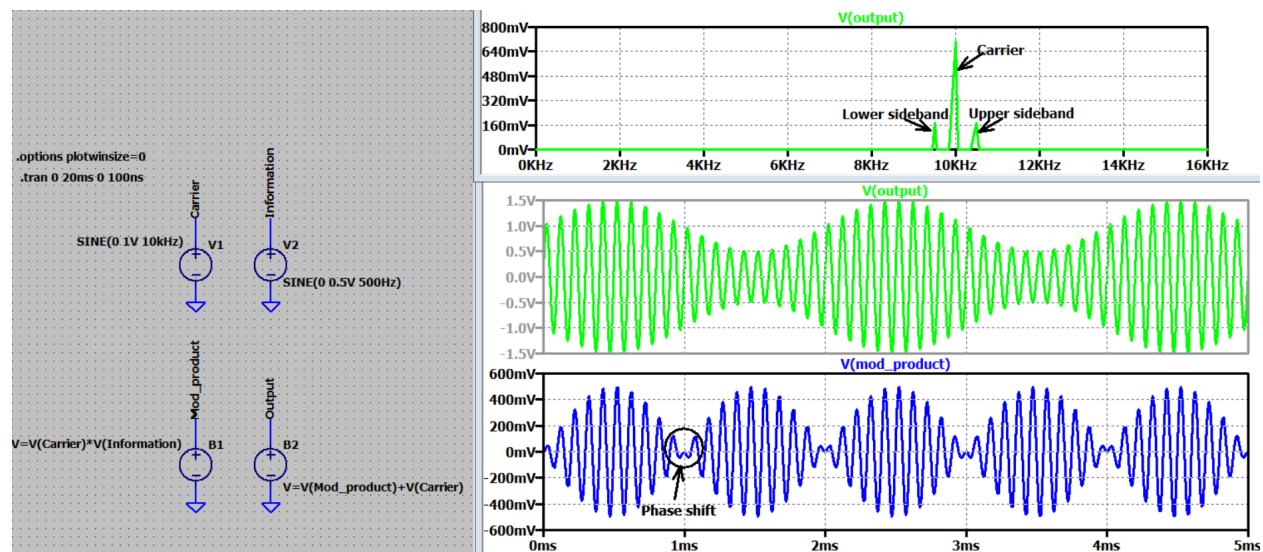


Figure 26: Amplitude modulation simulation scheme

Communication circuits simulation: Frequency modulation

In frequency modulation (FM) technique the carrier frequency is modulated in synch with the information signal [12]. In LTspice there is a single frequency FM (SFFM) source whereby a sinusoidal carrier is generated and sinusoidal information signal is automatically superimposed. Additionally, there is a complete FM-AM generator with a *modulate* function that can be found under the *Special Functions* section. Finally, the same FM-AM generator has a *modulate2* function that generates quadrature outputs [5]. The LTspice simulation of a basic FM signal is shown in Fig. 27 using the SFFM source with no dc component, a peak carrier value of 1 V, a carrier frequency of 10 kHz, a modulation index of 2π , and an information signal frequency of 1 kHz. If the carrier frequency increases it can be interpreted as advancing the phase in relation to the unmodulated signal. Similarly, a lower frequency means a reduction of the phase in relation to the unmodulated signal. The modulation index expresses this change of phase, and it represents the maximum phase shift in relation to the steady state with phase deviation measured

in radians. An FFT of the FM signal in Fig. 27 indicates that the entire spectrum is occupied with lines spaced at 1 kHz, the frequency of the information signal.

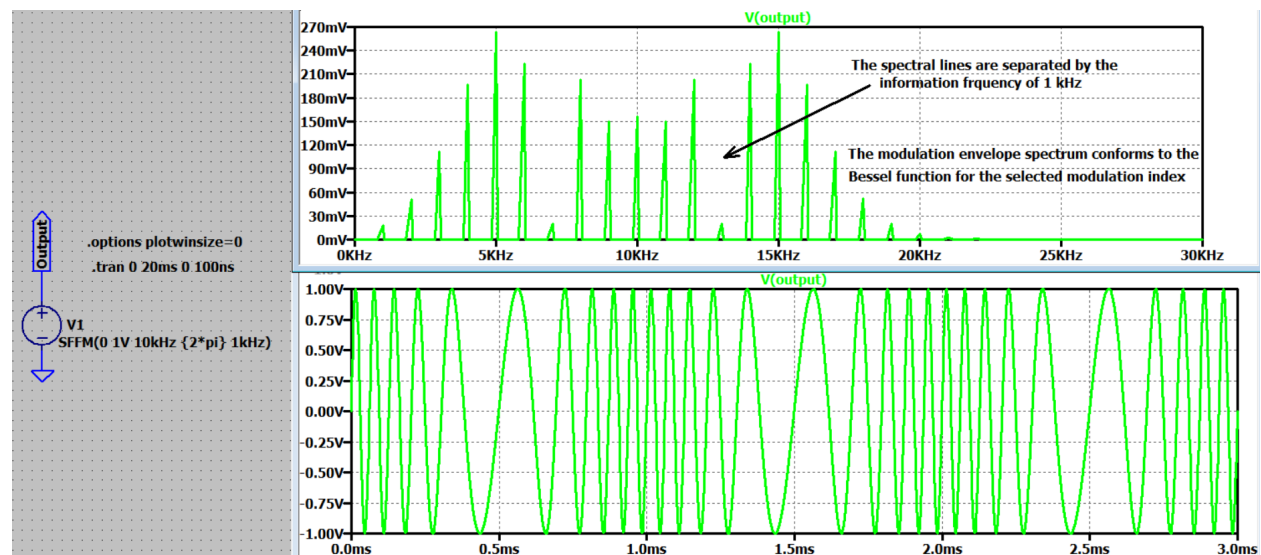


Figure 27: Frequency modulation simulation scheme

Communication circuits simulation: Ring modulator (Double balanced mixer)

Ring modulator, also called a double balanced mixer (DBM), is used for converting frequencies without changing the information content [12]. The two inputs are radio frequency (RF) signal of low amplitude (typically below 100 mV) and a local oscillator (LO) signal of high amplitude (typically a few volts). The output of the DBM is called the intermediate frequency (IF) output and this is the converted signal. Because of the multiplication of the RF and LO signals, the output of a DBM contains the sum and difference of the RF and LO frequencies. When using a square wave signal as the LO input, the signal consists of the fundamental frequency and the associated odd harmonics. This results in a DBM output consisting of a lot of signal pairs (sum and difference frequencies), and every pair is located at a harmonic frequency. In application circuits, a desired new frequency needs to be picked up with a lowpass or a bandpass filter.

The simulation schematic of a DBM using an ideal three-winding transformer [5] is shown in Fig. 28. The LO signal (a 1 MHz sine wave with a peak of 2 V) comes from the left and the RF signal (a 100 kHz sine wave with a peak of 20 mV) from the right. The simulated output (voltage across R3) in time domain as well as its FFT are included in Fig. 28. The polarity change of the RF signal caused by the LO signal can be clearly seen, however, the forward drop of the Schottky diode causes distortion at every zero crossing. Looking at the FFT plot it can be seen that at the fundamental frequency (1 MHz) as well as at every LO harmonic frequency a signal pair is present. Additionally, neither the RF signal nor the LO signal and its harmonics are present in the output.

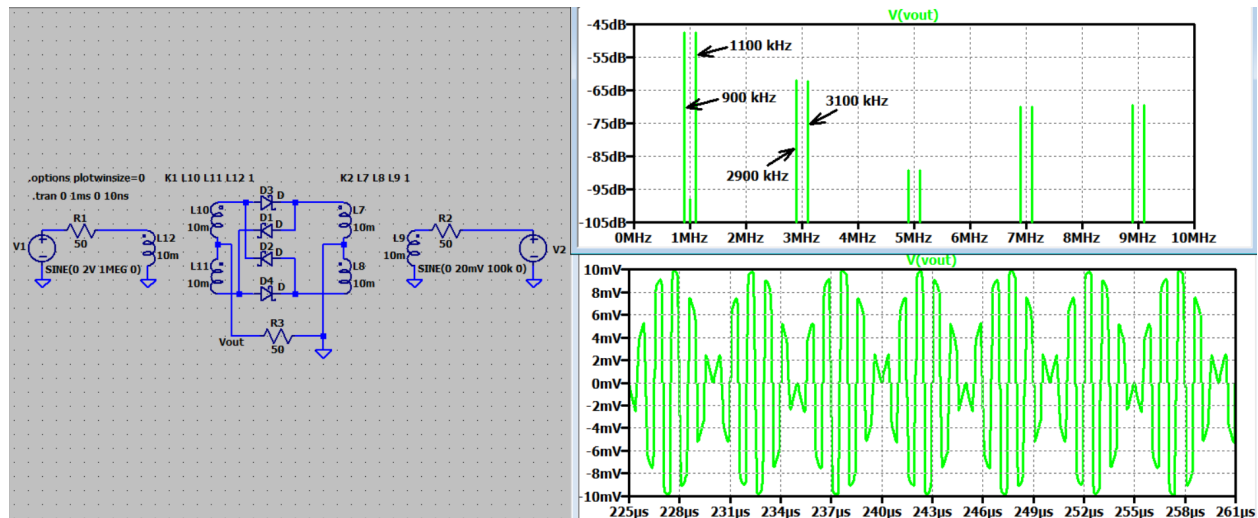


Figure 28: Simulation schematic for a double balanced mixer

Summary

The use of a free and full-featured circuit simulation software, suitable for face-to-face as well as remote instructional modes, is presented with several examples covering the areas of dc and ac circuits, analog and digital electronics, power electronics, differential equations, signals and systems, control systems, and communication systems. The presented use cases can be integrated into multiple EET courses, while supporting the ABET-ETAC student outcomes as well as EET type program criteria topics.

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