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RHL-BEADLE: Bringing Equitable Access to Digital Logic Design in Engineering Education

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Abstract

The vast scope of digital design and the cost associated with purchasing and maintaining specialized lab equipment can pose a significant obstacle for pre-college students. This challenge is particularly significant for students from low-income and underrepresented minority backgrounds who often begin their higher education journey in community college programs with limited funding and access to engineering hardware. BEADLE, a project designed to promote equity in access to educational technologies, seeks to address this issue by providing an affordable platform that allows students to remotely access industry-grade hardware to learn and develop their skills in digital design as a step towards pursuing advanced digital design coursework in a university setting. The success of an advanced digital design course delivered using a remote Field Programmable Gate Arrays (FPGA) lab inspired the creation of an introductory digital logic curriculum for 2-year community college and high school students. The BEADLE curriculum is designed to prepare students for a junior-level course in computer engineering at a 4-year university, where digital logic is typically taken during the first two years. To evaluate the curriculum, we offered it to a sophomore class on digital logic design at a 4-year public university and collected pre- and post-assignment surveys to gauge understanding of the material. Reflection pieces were also used to evaluate the students' approach and level of comprehension. In this paper, we provide an overview of the BEADLE curriculum, and report on the results of its evaluation using a remotely accessible FPGA lab. Additionally, we highlight the various features integrated into the remote lab platform, aimed at enhancing students' understanding of the curriculum content.

Introduction

The COVID-19 pandemic highlighted equity challenges for engineering students in remote learning, including limited access to suitable hardware and stable internet connections. Innovative solutions were needed to offer lab-based courses with strong learning outcomes to all students. Providing remote access to hardware was a cost-effective alternative to shipping laboratory kits worldwide and allowed for global access to a small number of hardware locations. Despite the perception of the remote lab approach as a temporary measure suitable only for the pandemic, our experience teaching a digital design course using a remotely accessible FPGA lab has proved successful in providing similar or even superior learning outcomes compared to traditional in-person labs [1]. This experience has inspired the development of the BEADLE curriculum, which leverages a remote FPGA lab to promote access to expensive, industry-grade hardware that could be out of reach for many underserved communities and educational institutions with limited budgets and resources.

The Remote Hub Lab (RHL or RHLab) [2] has developed RHL-BEADLE, a platform designed to introduce digital design to pre-college students by providing remote access to necessary hardware for laboratory assignments. Many students from lower-income and underrepresented minority backgrounds begin their college journey through community colleges [3]-[5] and seek to transfer to a four-year college to obtain a computer engineering degree. However, community colleges may face challenges in providing appropriate engineering coursework to align with

four-year university curriculums [6], such as a course on digital logic that is typically completed during freshman and sophomore years. This is due to the extensive breadth of the topic and the cost of supplying lab equipment to the community college and their students [7]. BEADLE intends to tackle this challenge by creating a series of laboratories that progressively cover the fundamental concepts of digital logic through a hands-on approach, utilizing remotely accessible FPGA hardware. The labs are structured to build upon each other gradually, enabling students to develop their knowledge and skills step-by-step, for comprehensive understanding of material.

BEADLE Curriculum & Features

The BEADLE curriculum consists of six labs that progressively cover digital logic concepts using hands-on approaches (figure 1). The curriculum requires no prior knowledge or experience in electrical engineering concepts.

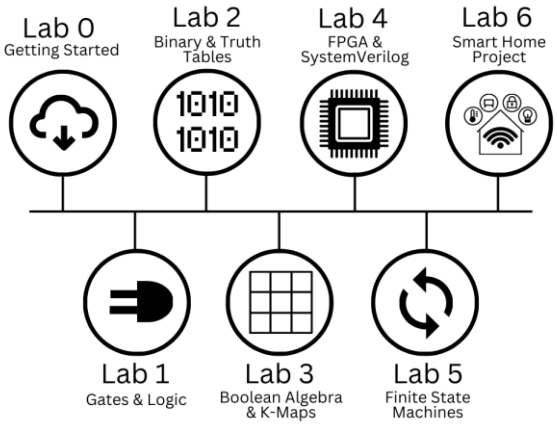


Figure 1: Organization of BEADLE labs

Lab 0 familiarizes students with the tools and technology used in the course, including software installations and remote lab platform accounts. Labs 1-3 build foundational knowledge of logic operators, gates, truth tables, and Karnaugh Maps. Labs 4-5 apply this knowledge to Hardware Description Language SystemVerilog and introduce sequential logic and Finite State Machines. Lab 6 is an independent project that culminates all the information provided in the course. The curriculum aims to provide a comprehensive understanding of programming an FPGA and distinguish it from programming a microcontroller using a high-level sequential programming language. Labs 4 and 5 aim to illuminate the essential characteristics of an FPGA, providing students with a clear understanding of this intricate technology within the curriculum.

The remote FPGA lab used in creating and testing this curriculum was hosted on campus [2], and students accessed it remotely from various locations. The lab used a distributed remote FPGA lab shared between 5 universities in 4 countries connected through a global network of remote laboratories called LabsLand [8]. Three main remote lab tools shown in Figure 2 are used in the BEADLE curriculum.

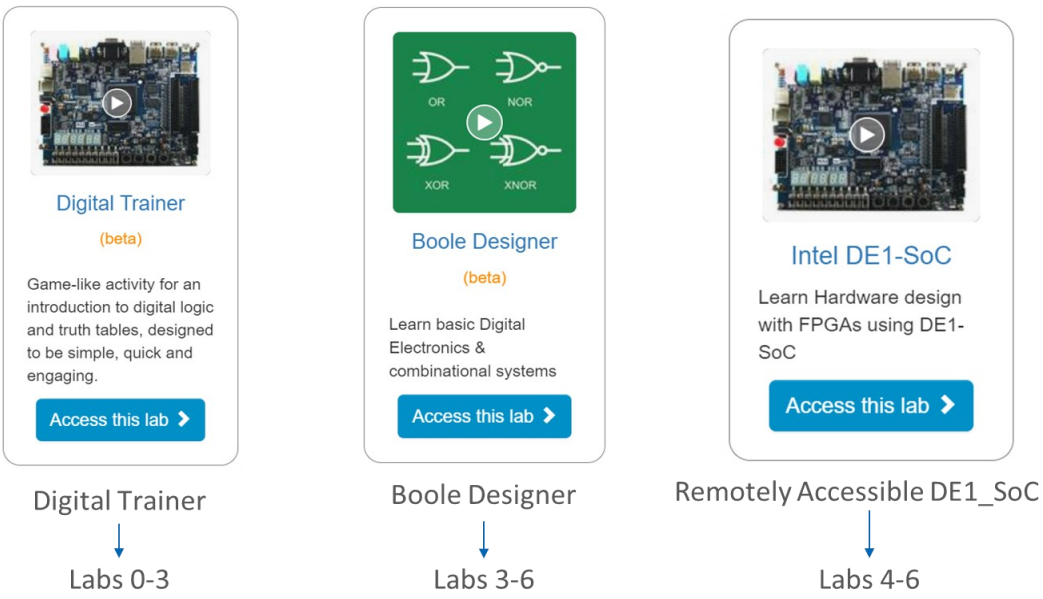
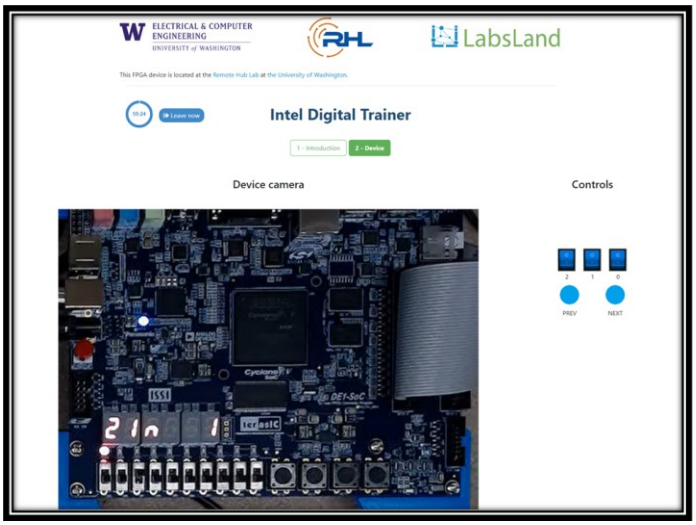
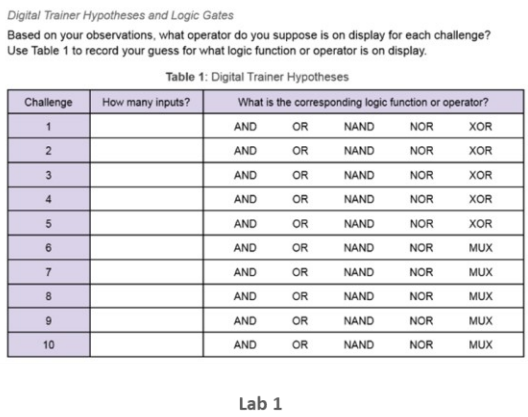


Figure 2: Tools used in respective BEADLE Labs

The Digital Trainer, shown in Figure 3, serves as the hardware platform for the initial four labs and presents a range of challenges supplemented by corresponding worksheet activities to engage students. The students can interact with the remote lab interface to manipulate inputs on the digital trainer and observe the output on the FPGA.





Digital Trainer Hypotheses and Logic Gates

Based on your observations, what operator do you suppose is on display for each challenge?
Use Table 1 to record your guess for what logic function or operator is on display.

Table 1: Digital Trainer Hypotheses

Challenge	How many inputs?	What is the corresponding logic function or operator?				
1		AND	OR	NAND	NOR	XOR
2		AND	OR	NAND	NOR	XOR
3		AND	OR	NAND	NOR	XOR
4		AND	OR	NAND	NOR	XOR
5		AND	OR	NAND	NOR	XOR
6		AND	OR	NAND	NOR	MUX
7		AND	OR	NAND	NOR	MUX
8		AND	OR	NAND	NOR	MUX
9		AND	OR	NAND	NOR	MUX
10		AND	OR	NAND	NOR	MUX

Lab 1

Figure 3: Digital Trainer tool

In Labs 3-6, the Boole Designer tool, shown in Figure 4, is utilized to aid students in comprehending the relationship between logic gates and Boolean expressions. Learners can generate their own truth table and employ a K-Map to visualize the Boolean expression, and the tool generates a circuit diagram as output. Several challenges embedded in this tool enable BEADLE users to construct parts of this progression solely based on a graphical representation.

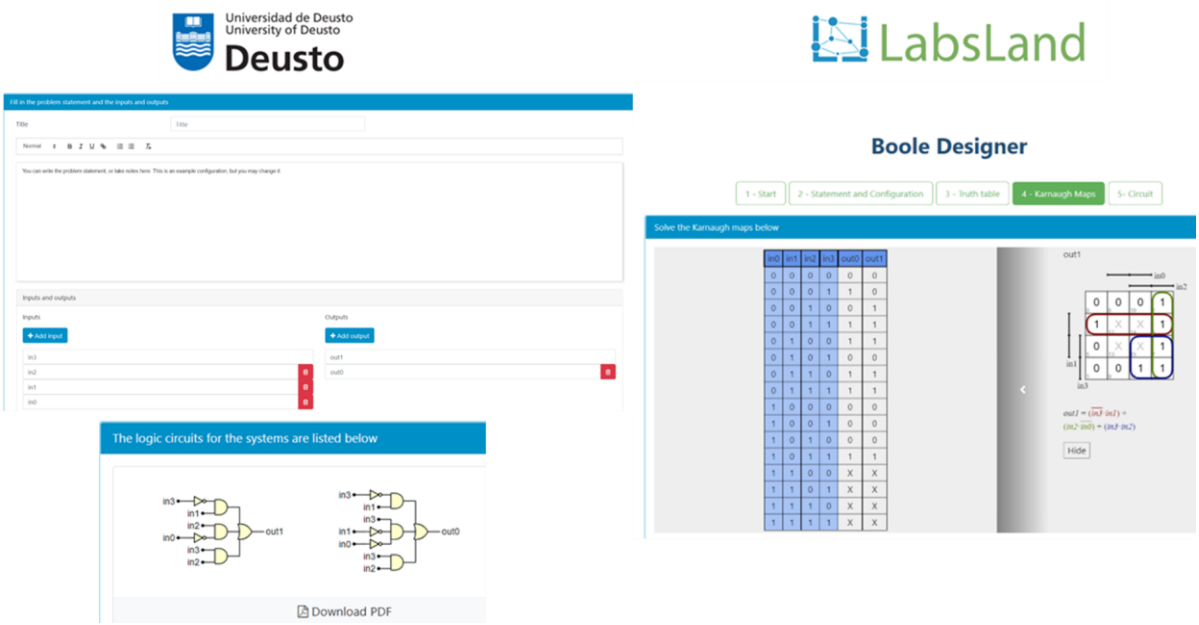


Figure 4: Boole Designer Tool

The BEADLE project utilizes the Remotely Accessible DE1-SoC, shown in Figure 5, as the final tool to enable students to create applications on real FPGAs. Through the remote lab interface, students can develop and synthesize their own SystemVerilog code, and then upload it over the internet to one of the boards available in the laboratory. Once an FPGA is reserved, students are given a specific amount of time to interact with the FPGA, manipulate the input controls on the board, and verify if the hardware configurations function properly.

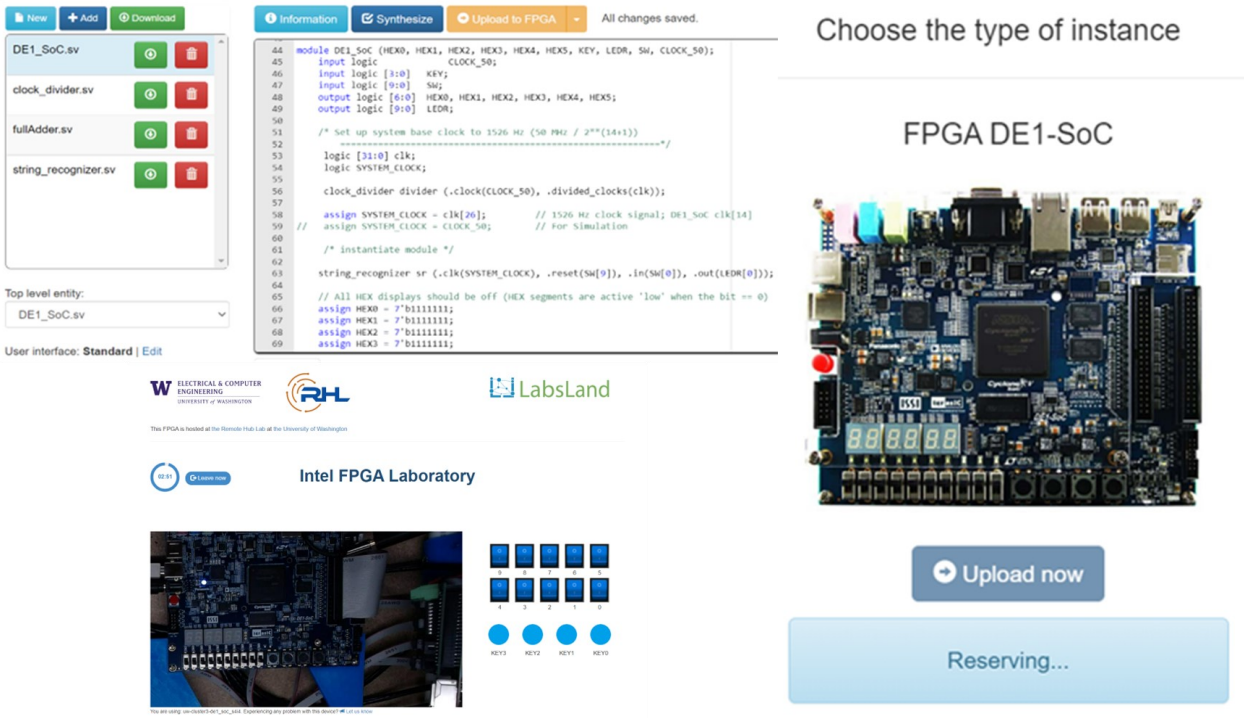


Figure 5: Remotely Accessible DE1-SoC

To the best of our knowledge, the Remote Hub Lab is known to be the largest remote Field-Programmable Gate Array (FPGA) lab to date, comprising 36 Intel DE1-SoC boards distributed across nine structures (Figure 6). Each structure is equipped with a camera that captures board peripherals and streams the information to a web interface, enabling students to synthesize and download their code to the FPGA. The lab is designed to be distributed, allowing students to access the boards at the Remote Hub Lab and other participating partner labs, such as the one in UPNA, Spain [9]. During the quarter when the curriculum was tested, 187 students enrolled in two digital design courses concurrently had access to the remote FPGA lab, resulting in 16,572 accesses to FPGAs. The lab experienced a median time of 5 seconds per session waiting for an FPGA board to become available, with an average of 5.70 and a standard deviation of 5 seconds. This type of experience has been analyzed in the literature [10]. Table 1 shows the distribution of students' sessions on the FPGA boards during that quarter, categorized by the time of day and day of the week. The data in the table indicates a surge in traffic on the remote lab around 23:00 pm, coinciding with the approaching deadlines of assignments.

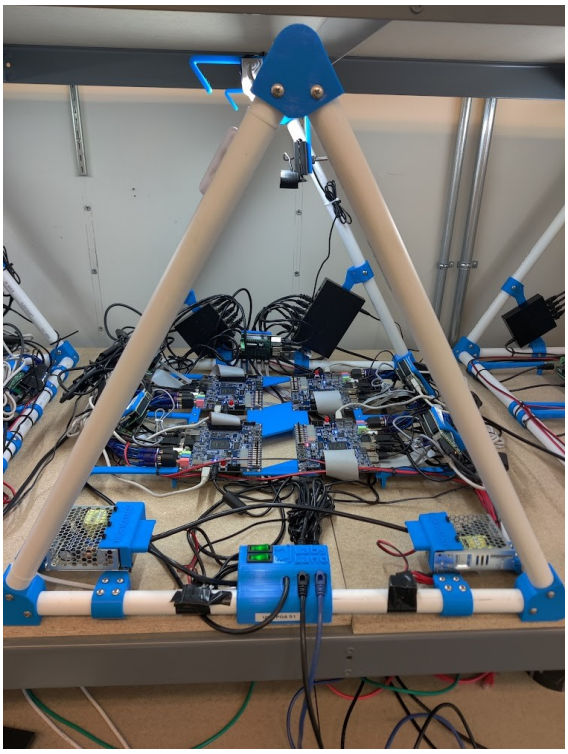


Figure 6: A structure that hosts 4 Intel’s DE1_SoC boards.

Student Access of FPGA's Through Week							
	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday	Sunday
0:00	71	104	79	97	62	89	69
1:00	44	39	37	58	84	62	42
2:00	40	26	26	33	67	48	32
3:00	11	2	22	17	40	20	33
4:00	29	6	15	11	21	17	15
5:00	7	12	9	6	22	2	17
6:00	0	12	0	16	11	3	9
7:00	15	34	10	13	9	5	9
8:00	22	32	18	24	14	22	3
9:00	36	29	41	40	29	18	23
10:00	38	52	58	59	58	17	57
11:00	96	32	116	114	70	53	146
12:00	91	59	108	125	69	45	141
13:00	105	51	166	156	118	83	144
14:00	114	96	187	182	153	89	128
15:00	128	89	245	145	201	75	216
16:00	167	94	231	147	233	57	256
17:00	148	138	179	192	266	66	273
18:00	167	122	163	202	219	98	305
19:00	194	80	148	127	245	94	225
20:00	200	90	183	191	245	115	261
21:00	226	125	190	200	220	119	303
22:00	251	180	263	164	175	184	279
23:00	240	129	173	161	111	115	204

Table 1: Activity on the remote FPGA lab grouped by day of the week and time of the day.

Boole-Web Implementation

As part of the BEADLE project, the open-source web software called "Boole-WebLab-Deusto" [11] was adapted to cater to the needs of the project. Originally based on "Boole-Deusto" [12], this tool allowed students to design lessons using Boolean algebra. With the adapted version, students can create problems, define inputs and outputs, and generate a truth table (shown in Figure 7) that can be used to visualize the corresponding K-Map and circuit (shown in Figure 8). Students can also assign inputs and outputs to an FPGA (as shown in Figure 9), generate VHDL code, and synthesize the code for later use on a real FPGA. The original "Boole-Deusto" [13] was more advanced and supported sequential assignments, including Finite State Machines.

To cater to the specific requirements of the BEADLE project, the Boole-WebLab-Deusto open-source web software needed to be adapted. Notably, the HDL language utilized in BEADLE is SystemVerilog, and the FPGAs used are as described in [2], necessitating seamless integration from the tool to the FPGA. Additionally, during the project's implementation, specific enhancements were identified and incorporated into the tool, which was renamed "Boole Designer" and included as part of its integration into BEADLE.

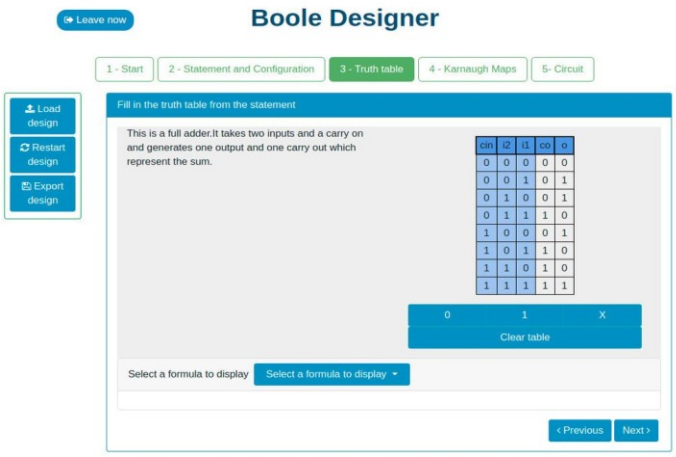


Figure 7: Constructing truth tables using Boole designer

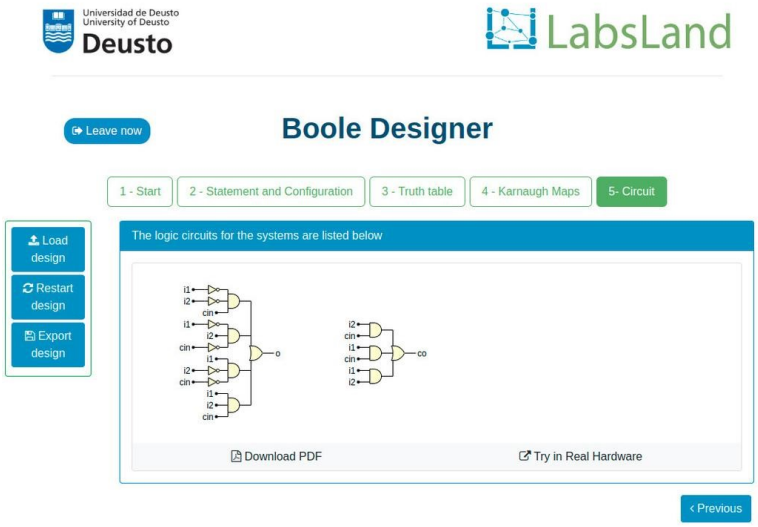


Figure 8: Transforming truth tables to circuit diagrams on Boole designer.

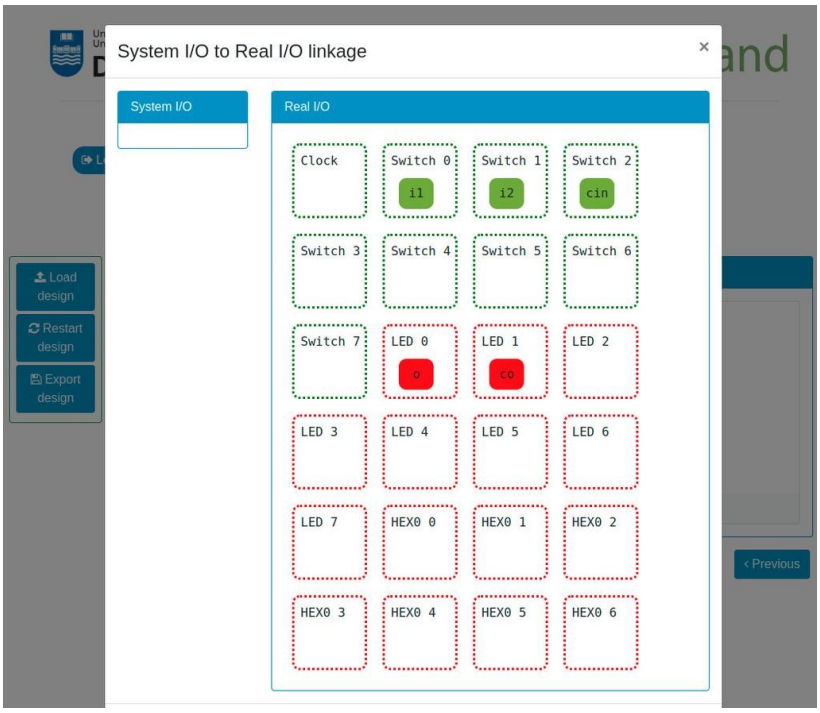


Figure 9: Mapping inputs and outputs (from truth tables) to switches and LEDs on the FPGA

The implementation of the Boole Designer included the following:

- In the Boole Designer, all files are automatically stored in the cloud. While users have the option to import and export designs, by default, their files are saved to their remote lab cloud accounts. This enables students to seamlessly access their latest designs from any web browser, including their phone or tablet, ensuring that they can easily resume their work.

- To facilitate the synthesis process and avoid the need for a powerful computer to download and synthesize code, the Boole Designer integrates with the LabsLand Compilation System, as shown in Figure 10. This system enables students to generate their code in the Boole Designer and then have it automatically synthesized and uploaded to the LabsLand ecosystem, even if they do not have access to a computer and are using only a mobile phone. To achieve this, multiple universities affiliated with LabsLand host software that downloads the tasks to be synthesized and then carries out the synthesis process. This approach shields students from the internal workings of the system, providing a seamless experience in which the HDL code they generate is synthesized remotely and made available within the LabsLand ecosystem.

- Within the framework of BEADLE, once the LabsLand Compilation System has synthesized the code produced from the truth table, students can transmit it automatically to a physical FPGA, without the need to download the file to their device or computer (as illustrated in Figure 11). Following this, students can interact with the circuit by operating the switches and observing the corresponding LED lights illuminated by the FPGA based on the values produced by their truth table.

Ultimately, numerous minor modifications were made to the initial Boole-WebLab-Deusto software to cater to the BEADLE curriculum. These alterations involved adjustments to the navigation process between phases and the support for both SystemVerilog and Verilog languages.

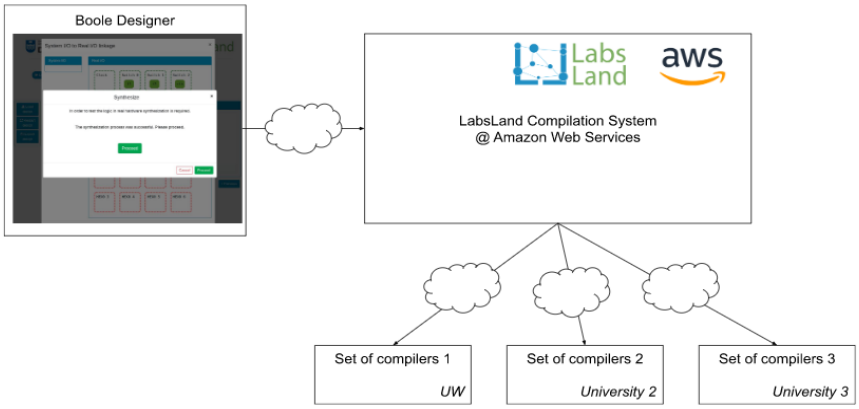


Figure 10: Integration on the LabsLand Compilation System

Figure 11: Real FPGA can be manipulated based on values present in a truth table.

To sum up, the Boole Designer tool enables educators to teach Boolean Algebra using a web application without requiring any plug-in installation within BEADLE. This platform facilitates students in creating a truth table, sending it to a real FPGA, and observing real-time interactions in just a few minutes.

Evaluation of BEADLE Curriculum

During the autumn quarter of 2022, a selection of modified BEADLE introductory labs was presented to a group of sophomore-level electrical engineering undergraduates enrolled in a

course on digital circuits and systems. It is noteworthy that the research conducted involved undergraduate students attending a four-year university rather than technical and community colleges. However, the population of students represented a diverse range of individuals from minority ethnic (Figure 12) and economic identities (Figure 13). The demographic data further revealed a strong presence of first-generation college students (Figure 14). To the best of our knowledge, the population bias was limited compared to that found in other educational institutions. Therefore, the results obtained from this evaluation are likely to be similar in other formal education settings.

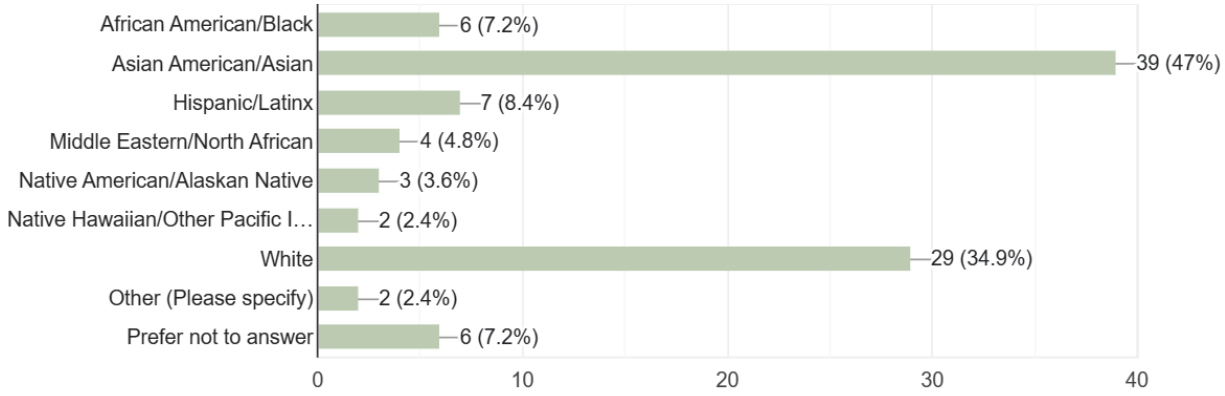


Figure 12: Bar chart showing racial and ethnic group population in the evaluation of BEADLE

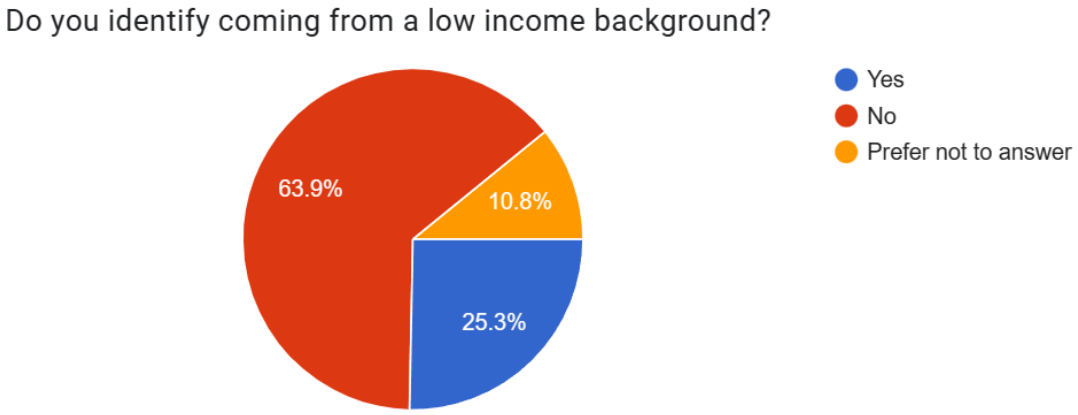


Figure 13: Pie chart showing low-income population in the evaluation of BEADLE

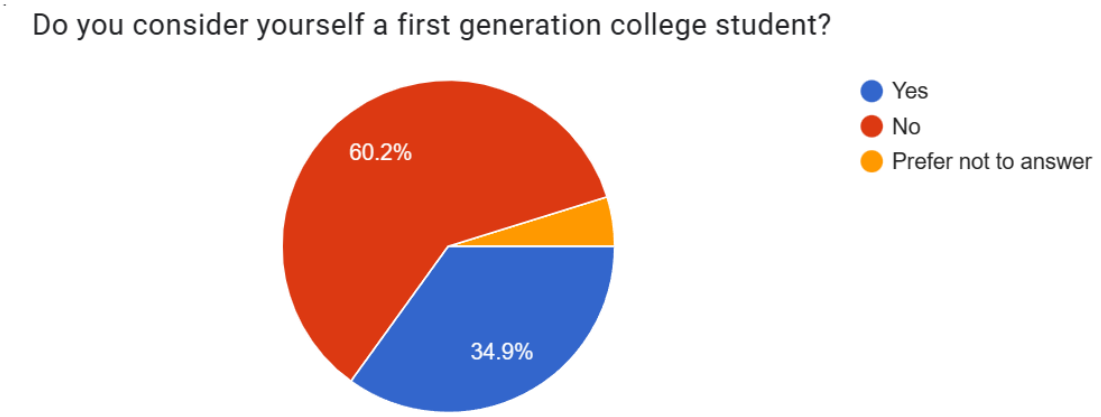


Figure 14: Pie chart showing first generation college population in the evaluation of BEADLE

These labs were assigned as two separate homework assignments. The first homework assignment covered topics in Lab 1, and the second assignment covered topics in Labs 2 and 3. Since the BEADLE curriculum was originally designed for pre-college students, the labs were modified to ensure that the content difficulty and guidance level were appropriate for university students. The purpose of introducing BEADLE to this population was to analyze whether the topics covered were suitable for underclassmen in university preparing for their in-major courses. Additionally, this presented an opportunity to evaluate the effectiveness of BEADLE and digital labs.

Self-Assessed Comfort

To evaluate the effectiveness and appropriateness of the BEADLE labs, pre- and post-lab surveys were administered to the students, a method that showed its effectiveness in literature [14]. Self-reporting of skills was used to gauge the students' comfort levels with specific digital logic topics. The survey used a rating scale from one to five, with one indicating "No Experience," and five indicating "Expert Understanding". Comfort with a topic has been found to have a strong correlation with a student's performance in that subject [15]. It is worth noting that students were encouraged to round up if they felt their skills and comfort levels were between two numbers, as many students who identify with Imposter Syndrome tend to underestimate their abilities [16]. Moreover, the Dunning-Kruger effect would be less prevalent because the population attended a competitive and advanced university [17]. Identical multiple-choice practice problems were also given to the students to answer. Aside from self-evaluation and multiple-choice questions, a self-reflection section was provided for students to participate in metacognition and consider their learning process. These responses allowed an opportunity to gather qualitative data on the developmental psychology of the population. A population of 82 students completed the surveys and consented to have their data released for research purposes.

Student learning was assessed through self-evaluation of comfort for skills in logic gates, logic operators, binary numbers, Boolean algebra, and K-Maps. Descriptive statistics for the scores are summarized in Table 2.

Change of Student Self-Identified Comfort of Topics While Using BEADLE												
1 - No Experience 5 - Expert Understanding												
Statistic	Logic Gates		Logic Operators		Binary Numbers		Truth Tables		Boolean Algebra		K-Maps	
	Before	After	Before	After	Before	After	Before	After	Before	After	Before	After
Mean	2.17	3.88	2.30	3.71	3.62	4.32	3.42	4.27	2.49	3.55	1.29	3.25
Median	2.00	4.00	2.00	4.00	4.00	4.00	3.50	4.00	2.00	4.00	1.00	3.00
Standard Deviation	0.97	0.69	1.04	0.71	0.83	0.68	1.00	0.59	0.87	0.68	0.62	0.86
Skew	0.32	-0.95	0.22	-0.18	-0.28	-0.77	-0.43	-0.12	0.35	-0.26	1.98	0.07
Kurtosis	-0.93	3.09	-1.13	-0.15	0.21	0.45	-0.04	-0.48	-0.16	-0.10	4.09	-0.18

Table 2: Comfort of topic data from survey results

Through almost all measured skills, the skewness of the data lies in the standard range between -1 and +1, thus [18]. For the occurrences when the value came close to or passed this threshold, the median and mean scores were on the extreme ends of the rating scale. This would also appear natural since there is little room for symmetry on a distribution that gets cut off short by a limit on one side. The kurtosis values tended to be lower than the typical normal distribution of 3 [18]. This was also to be expected as the measurements for the data did not have intermediate values (such as 2.5), which would cause a broad peak. Overall, the method used to analyze student learning was consistent with natural occurrences of probability and is appropriate to use to identify the effectiveness of BEADLE.

Topics that heavily relied on support from BEADLE hardware (including logic gates, logic operators, and K-Maps) demonstrated the most improvement. This is seen by looking at the change of mean comfort before and after the same subject. For example, logic gates had an initial average comfort level of 2.17, but this value was increased to 3.88 after using the BEADLE curriculum. One outside factor to this could have been that these topics had the lowest initial comfort scores, causing more room for growth in the subject matter. Having most of a cohort migrate from having minimal knowledge of a topic to creating self-identified aptitude can only come from an effective learning development context. The mean comfort level after BEADLE for all the topics collectively revolved around a score of 4, which would signify students feel they have a strong understanding of digital logic and could perform applications of said topics with consistent correctness. In opposition, before BEADLE, the median collectively was 2 for many topics, suggesting students initially felt ill-prepared in the subject matter and had limited prior knowledge. This collectively indicates the effectiveness of the BEADLE curriculum and remote hardware labs.

Multiple-choice Questions

In the multiple-choice section of the surveys, there was strong evidence that the BEADLE curriculum positively impacted students' learning. All the multiple-choice questions had a higher rate of correct answers after using the BEADLE labs. Moreover, every question had higher than

80 percent correctness for post-lab surveys. The results of the self-identified assessment were verified by analyzing results from multiple-choice questions.

The first question was Figure 15 A, which evaluated students' knowledge of identifying drawn logic gates. Surprisingly, 67 percent (Table 3) of students could identify the correct logic gate the first time without using the BEADLE curriculum. This stemmed from the fact that students had briefly covered this material in the lecture before completing the assignment. Nearly the entire test population selected the answer correctly the second time, as 99 percent chose the correct solution.

The question from Figure 15 B tests students' knowledge of Boolean operator symbols, which is similar to the logic gate identification question. Forty-three percent (Table 3) of the students got the question correctly the first time as XOR. A common misconception was when 31 percent of students decided to pick the AND operator. This was mainly because the XOR operator has a similar symbol as the additives used in normal algebraic notation. The correct number of answers doubled to 88 percent (Table 3) after using the BEADLE project, proving students could understand the reasoning for their misidentification.

Figure 15 C shows a question that had the most dramatic change in percentage was a question on identifying logic gates. The results from the pre-assessment had a relatively even distribution across all potential options. The correct answers for this question were when AND and OR were selected. In determining the correct answers, the selection (or lack of selection) for MUX was ignored. The correct response rate shifted from 39 to 85 percent (Table 3) before and after using the BEADLE curriculum, respectively. This indicates that the population that identified logic gates correctly doubled in size. Additionally, more than half of the remaining 15 percent of the population with the wrong solution after the BEADLE curriculum could identify at least one of the correct gates.

Question D from Figure 15 marks the first question in the second homework assignment. This question had lots of overlap in content with the first lab presented, which made this a question based on retention of knowledge. Ninety-one percent of students remembered how an XOR operator works, and that number rebounded to 97 percent after the assignment was completed. This question was important in identifying that students can retain information gathered from the BEADLE project over multiple weeks rather than right after completing the assignment.

Another question was asked to identify DeMorgan’s Law, as shown in Figure 15 E. During the pre-assessment, 58 percent of the students correctly identified the option explaining that “Negating an entire operation is the same as negating each signal and changing to the opposite operator.” Most alternate options explained other laws or functions corresponding to basic algebraic operations. After going through the BEADLE curriculum, 87 percent of students could identify the correct explanation of DeMorgan’s Law which improved from the original 58%.

Finally, students were asked to identify the proper algebraic formula that would result in a K-Map, as shown in Figure 15 F. While 42 percent of students identified the second option as correct in the pre-assessment, all other options were selected by around an equal 20 percent. In the post-survey, 83 percent of the students identified the correct answer, with all but one of the

remaining students choosing a similar option that used the "*" operator instead of the "+" operator.

Changes in Student Survey Multiple-Choice Questions						
	Percent Correct Response					
Time Taken	Question A	Question B	Question C	Question D	Question E	Question F
Before	67%	43%	39%	91%	58%	42%
After	99%	88%	85%	97%	87%	83%

Table 3: Multiple-choice Correct Response Data

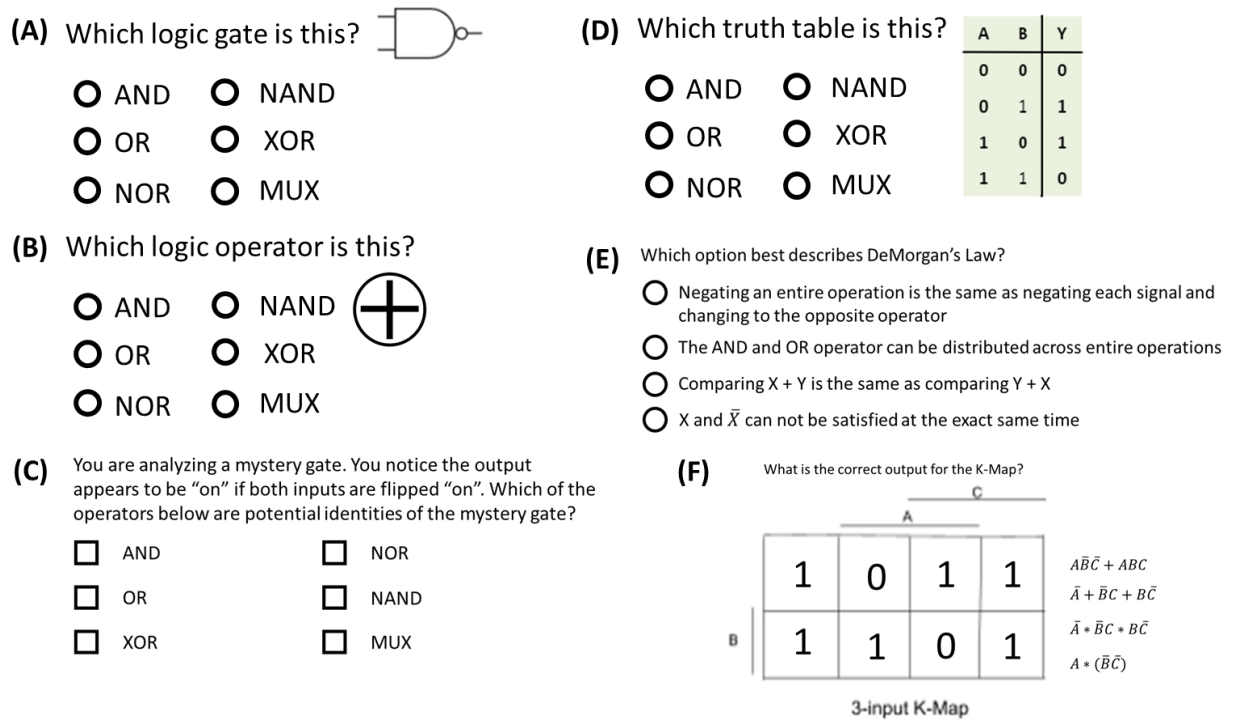


Figure 15: Multiple-choice questions on pre/post-surveys

Looking over the multiple-choice section of the survey, it is fair to say that the students' self-evaluation of comfort and skill was well reflected by their actual application and performance or equivalent topics. Through the entire curriculum, the population as a whole was able to improve their understanding of various topics covered in the BEADLE curriculum. This likely came from the ability of the students to visualize their work through worksheets provided by the labs and the ability to apply and explore their learning on actual FPGA boards supplied through the internet. Providing an accessible way to perform kinesthetic learning most likely helped a population of students develop and learn in a form that is typically underrepresented with university and college curricula. These results indicate that the BEADLE curriculum created a learning environment that successfully promoted student understanding of digital logic. The opportunity

for students to interact with FPGAs and other tools remotely did not hinder but accelerated the learning process among students at the university level.

Reflection Questions

Students were asked in their post-lab survey to share, "What were your biggest stumbling points for you during this assignment?" As seen in Figure 16, a large population mentioned K-Maps as being one of the hardest things to comprehend.

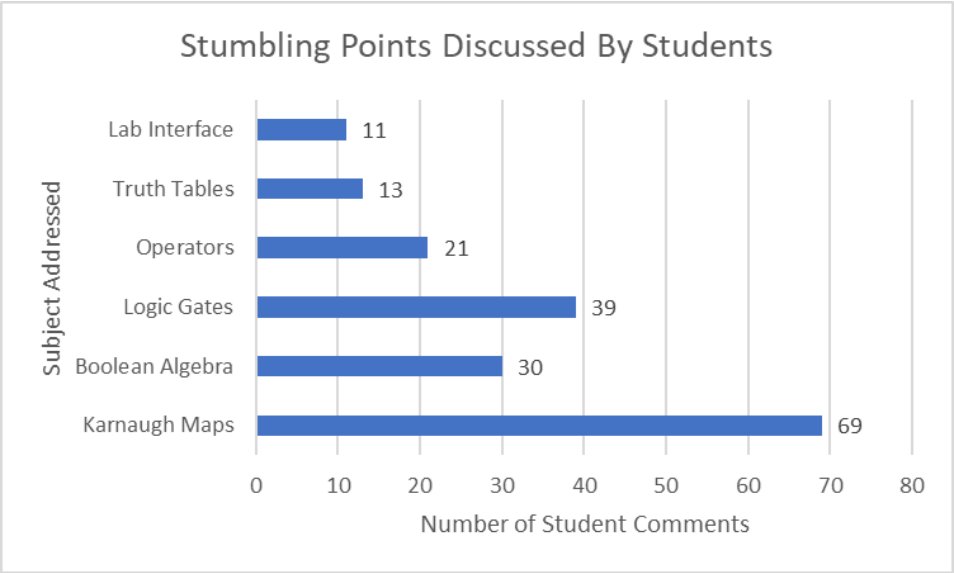


Figure 16: Reflection topic data on student stumbling points

Over half of these comments continue to mention they could not translate groupings into boolean logic. A larger story is in place when understanding digital logic with more than two inputs. Many students made comments surrounding the opinion that "It was hard to understand K-maps" because "[they] are so dense" and difficult to read. Moreover, when first introduced to multiplexers, the students also identified a common struggle to interpret outputs since they "didn't feel as intuitive as other logic gates" since they had multiple inputs. The majority of students, when addressing logic gates, tend to comment specifically on multiplexers as they were rarely a part of the students' toolkit of prior knowledge. With this, an overarching theme is determined that problems get increasingly difficult to interpret as more variables are measured at the same time.

While it is intuitive that problems with more factors will create greater difficulty, students noted how the BEADLE features on the remote lab platform helped them become more familiar with the topic. Students reported their use of the remote lab when reinforcing their learning after the lesson. Figure 17 summarizes the results from a short response asking students, "How do you plan to reinforce what you have learned from this assignment?"

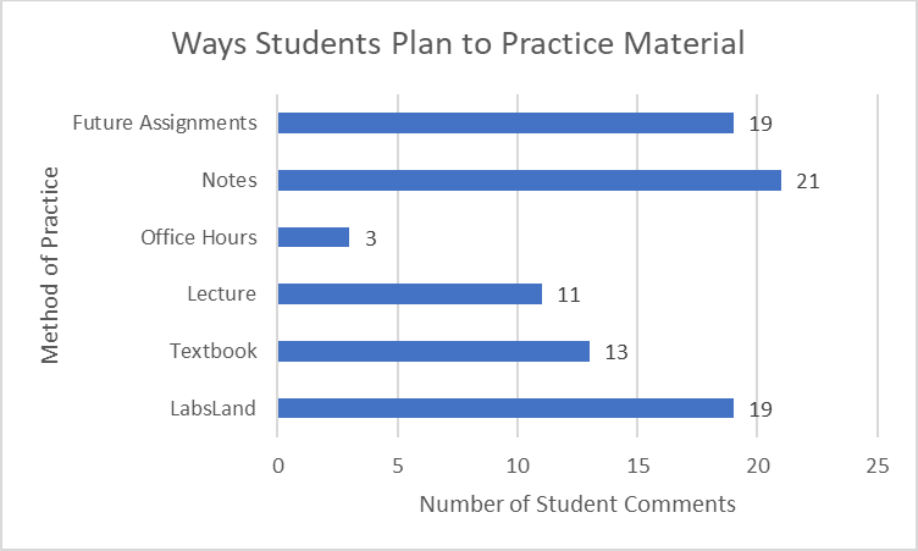


Figure 17: Reflection topic data on how students plan to reinforce learning.

19 students brought up how they would continue to use the remote lab resources to strengthen their learning. The size of this population was similar to those who wanted to refer to their notes, 21 students, or work on future assignments, 19 students. These students overwhelmingly acknowledge that the BEADLE curriculum tools were critical in their learning development. A few students mentioned using the "LabsLand boolean algebra tool" to "practice converting to and from gates, algebra, and K-Maps." It is important to note that other students mentioned using online lectures, textbooks, professors, and other resources as different ways to reinforce their learning. A large population found the remote lab resources an effective way to fortify their learning just as much as other traditional methods.

As seen in Figure 16, a small population of 11 students did bring up notes that the remote lab platform interface had a slight learning curve. That said, the effort to become familiar with the program was much smaller than learning the material in the curriculum. Additionally, students noted how fascinating it was to be interacting with real-life hardware. Because there was overwhelming evidence that the student population found the program useful, it could be interpreted that any learning curve experienced using this technology was an investment into their learning, like any other topic or lesson. One student mentioned how after they took a few moments to understand "the controls [on the remote lab] the assignment went pretty easy." Overall, our results show that the BEADLE curriculum created a new way for students to continue their learning of digital logic. This was demonstrated with integrated lessons and practice problems, which could seamlessly intertwine with other curriculums and resources provided to learners.

Students Feedback

Notably, the students in the sophomore class, where BEADLE was implemented, were introduced to remote FPGA technology for the first time during the course. At the conclusion of the course, we conducted an anonymous survey to collect their feedback on their experience with the remote hardware. The results, as illustrated in Figure 18, were overwhelmingly positive, with 83 out of 85 total enrolled students responding to the survey.

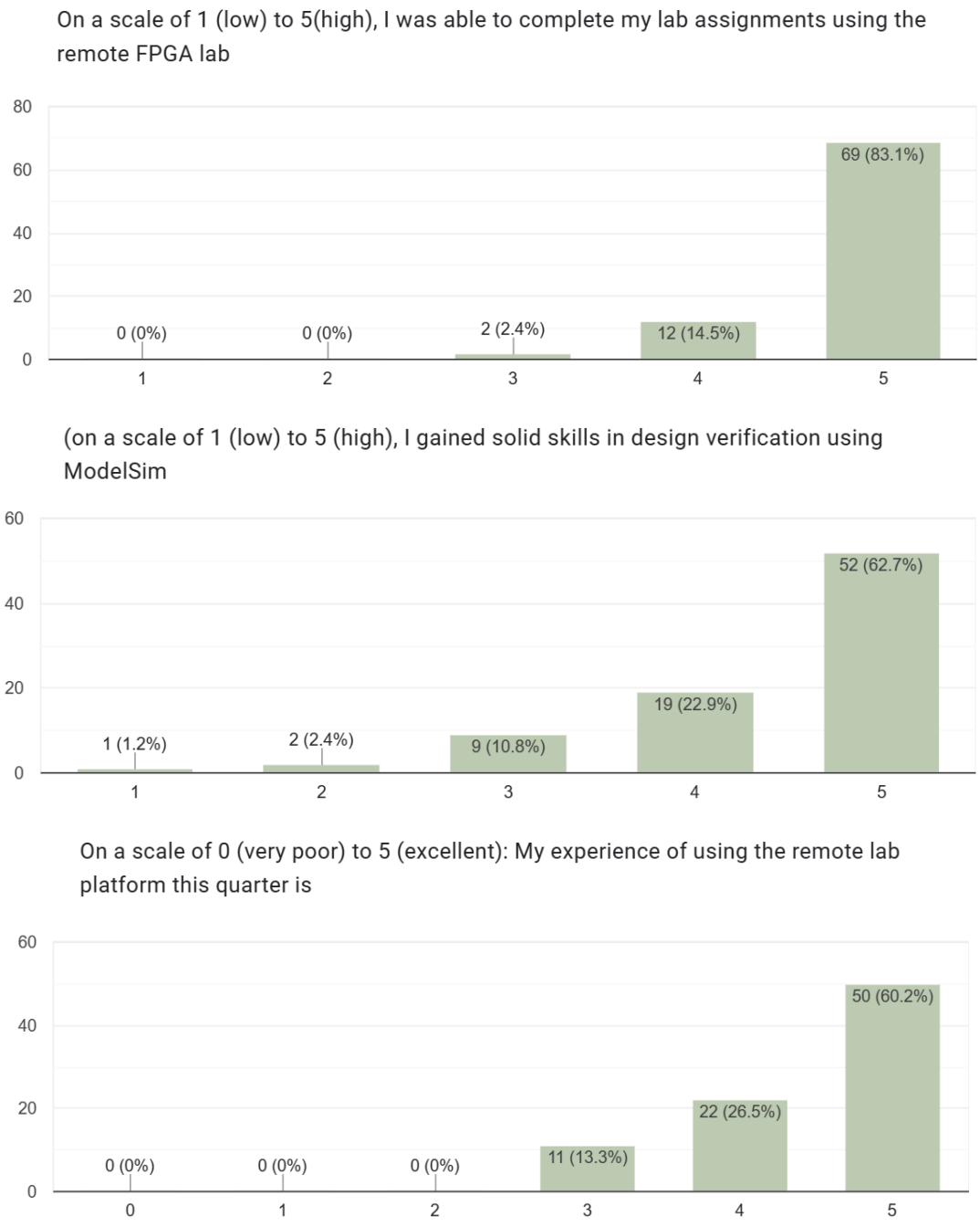


Figure 18: Results of an anonymous survey that assessed the opinions of sophomore students regarding their usage of the remote FPGA lab to complete laboratory assignments.

This demonstrates that the remote lab would be a suitable and cost-effective option for pre-college students to gain access to industry-grade hardware. Educators from community colleges and pre-college institutions who incorporate BEADLE into their curriculum would be granted access to the remote FPGA lab at a reasonable subscription fee compared to buying, distributing, and maintaining hardware. This easily accessible solution is predicted to increase involvement

from institutions serving a significant number of underrepresented students or those in underprivileged communities.

Conclusion and Future Work

This paper's findings suggest that BEADLE positively impacted students' understanding of electrical engineering concepts, as shown by pre- and post-assignment surveys and reflection questions. This supports the potential of remote laboratory-based education as a viable option. While our assessment of the BEADLE curriculum only covers a portion of its content, the outcomes thus far demonstrate its potential in effectively promoting engineering design to pre-college students. Nevertheless, conducting a comprehensive evaluation in an authentic pre-college setting would be a logical progression to inform the refinement of the curriculum to cater to a diverse range of learners.

BEADLE was initially developed to create a digital design curriculum for pre-college students utilizing remotely accessible FPGAs, but with the addition of other hardware and development boards, its scope is expanding to provide more opportunities for its audience [2]. The RHL-Butterfly project [19], which integrates breadboards for circuit building with FPGA boards and microcontrollers, will increase BEADLE's subject outreach, providing more opportunities for current and future partners. As BEADLE evolves to serve the public, future efforts will include monitoring the effectiveness of the curriculum, developing unique labs for various experience levels, and promoting the learning resource to underserved populations. This project has the potential to serve as an effective tool for promoting equity in the field of electrical engineering education. Its expansion to serve a broader audience and provide more opportunities for learning will be essential in bridging the technology and education gap that exists within marginalized communities. Therefore, our future efforts will seek partnerships with community colleges and educators to develop hybrid learning models and promote fundamental digital design in K-12 curriculums and extracurricular activities.

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